Printed Circuit Board Decoupling

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The Concept of Power Bus Decoupling

[Diagram showing a printed circuit board and a power supply with inductance marked as $L_P$ and $L_G$.]
The Concept of Power Bus Decoupling

Printed Circuit Board

Power Supply

\[ V_{\text{board}} \]

\[ V_{\text{supply}} \]

\[ L_P \]

\[ L_G \]
The Concept of Power Bus Decoupling
Why is this a problem?

Signal Integrity is compromised!

Power Bus Noise ➔ Radiated and Conducted EMI!
Why is this a problem?

For some ICs, the high-frequency currents drawn from the power pins can be much greater than the high-frequency currents in the signals!
Has anybody studied this?


A lot of people have been looking at the power bus noise problem for a long time.

John R. Barnes’ Bibliography has 837 entries.
Conflicting Rules for PCB Decoupling

Use small-valued capacitors for high-frequency decoupling.

Locate capacitors near the power pins of active devices.

Avoid capacitors with a low ESR!

Run traces from device to capacitor, then to power planes.

Location of decoupling capacitors is not relevant.

Use the largest valued capacitors you can find in a given package size.

Use 0.01 μF for local decoupling!

Use capacitors with a low ESR!

Use 0.001 μF for local decoupling!

Locate capacitors near the ground pins of active devices.

Never put traces on decoupling capacitors.

Local decoupling capacitors should have a range of values from 100 pF to 1 μF!
Main Questions

- How much capacitance do I need?
- Where should it be located?
- How should it be connected?
Conflicting Goals?

- Do we want a low-impedance power bus that can supply lots of current without a significant change in voltage?

- Do we want a high-impedance power bus that isolates each device from other devices?
How much capacitance do you need?

\[ V_{\text{NOISE}} = Z_{\text{SUPPLY}} \cdot I_{\text{DEVICE}} \]
How much capacitance do you need?

\[ Z_{\text{max}}(f) = \frac{V_{\text{NOISE MAX}}(f)}{I_{\text{DEVICE MAX}}(f)} \]

\[ \frac{1}{2\pi f_0 C} = Z_{\text{max}} \]

\[ C_{\text{min}} = \frac{1}{2\pi f_0 Z_{\text{max}}} \]

\[ f_0 = \frac{Z_{\text{max}}}{2\pi L_{\text{source}}} \]

Printed Circuit Board

Power Supply

\[ L_p \]

\[ L_g \]

\[ V_{\text{board}} \]

\[ V_{\text{supply}} \]
How much capacitance do you need?

Impedance approach

\[ Z_{\text{max}}(f) = \frac{V_{\text{NOISE MAX}}(f)}{I_{\text{DEVICE MAX}}(f)} \]

\[ \frac{1}{2\pi f_0 C} = Z_{\text{max}} \]

\[ C_{\text{min}} = \frac{1}{2\pi f_0 Z_{\text{max}}} \]

\[ = \frac{1}{(2\pi f_0)^2 L_{\text{source}}} \]
Recognizing that CMOS loads are capacitances, we are simply using decoupling capacitors to charge load capacitances.

Total decoupling capacitance is set to a value that is equal to the total device capacitance times the power bus voltage divided by the maximum power bus noise.
How much capacitance do you need?

Guidelines approach

Let’s do it the way that worked for somebody at sometime in the past.

“... include one 0.01 uF local decoupling capacitor for each VCC pin of every active component on the board plus 1 bulk decoupling capacitor with a value equal to 5 times the sum of the local decoupling capacitance.”
Main Questions

- How much capacitance do I need?
- Where should it be located?
- How should it be connected?
Printed Circuit Board Decoupling Strategies
Boards without Power Planes

OK?
Boards without Power Planes

Got a ground plane?
The effectiveness of a single capacitor as a filter is limited by mutual inductance.
Two capacitors can be much more effective than one.
With no power plane

- layout low-inductance power distribution
- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- two caps can be much better than one
- avoid resonances by minimizing L

References:


Boards with Closely Spaced Power Planes

Power Distribution Model ~ (5 - 500 MHz)
Board with power and ground planes
Boards with Closely Spaced Power Planes

\[ C_B = 3.4 \text{ nF} \]
\[ L_{\text{BULK}} = 5 \text{ nH} \]
\[ L_D = 2 \text{ nH} \]
\[ C_{\text{BULK}} = 1 \mu \text{F} \]
\[ C_D = 10 \text{ nF} \]

\[ |Z| \text{ in ohms} \]

0.1 MHz 1 MHz 10 MHz 100 MHz 1 GHz

Bare Board
Board with decoupling
For Boards with “Closely-Spaced” Planes

- The location of the decoupling capacitors is not critical.
- The value of the local decoupling capacitors is not critical, but it must be greater than the interplane capacitance.
- The inductance of the connection is the most important parameter of a local decoupling capacitor.
- None of the local decoupling capacitors are effective above a couple hundred megahertz.
- None of the local decoupling capacitors are supplying significant charge in the first few nanoseconds of a transition.
On boards with closely spaced power and ground planes:

Generally speaking, 100 decoupling capacitors connected through 1 nH of inductance will be as effective as 500 decoupling capacitors connected through 5 nH of inductance.
With closely spaced (<.25 mm) planes

- size bulk decoupling to meet board requirements
- size local decoupling to meet board requirements
- mount local decoupling in most convenient locations
- don’t put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

References:


Boards with Power Planes Spaced >0.5 mm
4-Layer Board Measurements
4-Layer Board Measurements

![Graph showing measurements of 4-layer board with different conditions.](image)
Boards with Power Planes Spaced >0.5 mm

On boards with a spacing between power and ground planes of ~30 mils (0.75 mm) or more, the inductance of the planes can no longer be neglected. In particular, the mutual inductance between the vias of the active device and the vias of the decoupling capacitor is important. The mutual inductance will tend to cause the majority of the current to be drawn from the nearest decoupling capacitor and not from the planes.
Where do I mount the capacitor?
4-Layer Board Measurements

$|S_{21}|$ With Capacitor Sharing One Pad With Port 1

- Blue line: probe 1 and 0.1 µF cap., share power pad of CSL3
- Red line: probe 1 and 0.1 µF cap., share ground pad of CSL3
- Green line: 0.1 µF cap. at CS4H3, far from probes

- Active Device
- Decoupling Capacitor

Signal Layer
Return Plane
Power Plane
Signal Layer
Active Device
Decoupling Capacitor
Signal Layer
Return Plane
Power Plane
Signal Layer

T. Hubing
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Local decoupling capacitors should be located as close to the active device as possible (near pin attached to most distant plane).

The value of the local decoupling capacitors should be 10,000 pF or greater.

The inductance of the connection is the most important parameter of a local decoupling capacitor.

Local decoupling capacitors can be effective up to 1 GHz or higher if they are connected properly.
Power Bus Decoupling Strategy

With widely spaced (> .5 mm) planes

- size bulk decoupling to meet board requirements
- size local decoupling to meet device requirements
- mount local decoupling near pin connected to furthest plane
- don’t put traces on capacitor pads
- too much capacitance is ok
- too much inductance is not ok

References:


Power Bus Resonances

What happens here?
Power Bus Resonances

No excitation

$\text{TE}_{10}$

$\text{TE}_{20}$

$\text{TE}_{44}$
Input impedance of an unpopulated 2” x 3” FR4 board with 22-mil power/ground plane spacing
Power Bus Resonances

Input impedance of a populated 8” x 9” FR4 board with closely spaced (4.5 mil) planes
Input impedance of a populated 2” x 3” board with embedded capacitance

![Graph showing input impedance over frequency](image)
## Do you need Power Planes?

<table>
<thead>
<tr>
<th>Advantages of power planes</th>
<th>Disadvantages of power planes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Provides high-frequency current</td>
<td>Lower power bus impedance may increase current rise in devices, leading to stronger RF and EMI</td>
</tr>
<tr>
<td>Lower power bus impedance reduces noise voltage on power bus</td>
<td>Possibly higher layer count.</td>
</tr>
<tr>
<td>Easier to route power</td>
<td>Power bus resonances may radiate directly from the plane pair.</td>
</tr>
<tr>
<td>Large current handling ability</td>
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Do you ever want a higher power bus impedance?

If planes are used, but components are not connected directly, then a connecting impedance (e.g., a small resistor or a ferrite bead) can be used to decouple the IC from the plane, or, to decouple the plane from the IC.

A local decoupling capacitor can be placed on the device side of the connecting impedance

BUT …
Do you ever want a higher power bus impedance?

DON’T CUT OR “MOAT” THE GROUND PLANE!
Low-impedance planes or traces?

- choice based on bandwidth and board complexity
- planes are not always the best choice

Planes widely spaced or closely spaced?

- want local or global decoupling?
- want stripline traces?
- lower impedances obtainable with closely spaced planes.
In order to be effective, capacitors must be located within a radius of the active device equal to the distance a wave can travel in the transition time of the circuitry.

On boards with closely spaced planes (where this rule is normally applied) none of the capacitors on the board can typically respond within the transition time of the circuitry no matter where they are located.
Smaller valued capacitors (i.e. 10 pF) respond faster than higher valued capacitors.

The ability of a capacitor to supply current quickly is determined by its mounted inductance. The value of the capacitance only affects its ability to respond over longer periods of time. For a given value of inductance, higher valued capacitors are more effective for decoupling.
Active devices should be connected with traces to the capacitor, then through vias to the power planes.

This sounds like a good idea until you apply some realistic numbers and evaluate the tradeoffs. In general, any approach that adds more inductance (without adding more loss) is a bad idea. Power and ground pins of an active device should generally be connected directly to the power planes.
Final Words

- Correct strategy depends on plane spacing!
- PCB Decoupling is mostly about capacitance at kHz frequencies
- PCB Decoupling is mostly about inductance at MHz frequencies
- PCB Decoupling is mostly non-existent at GHz frequencies