

## **TECHNICAL REPORT: CVEL-10-018**

### **A Novel Balanced Cable Interface for Reducing Common-Mode Currents from Power Inverters and Other Electronic Devices**

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## Abstract

Common-mode current is a significant source of radiated emissions from power inverters. In an ideal power inverter, the currents flowing in one direction on the wires between the inverter and the load are exactly equal to the currents flowing in the opposite direction in the same wire bundle. Unfortunately, imbalances in the switching components and circuit geometry can cause the electrical potential of the wire bundle to change with time resulting in common-mode currents. Most inverters employ pulse-width modulated switching at frequencies below 100 kHz. Balancing an inverter at low frequencies without affecting the performance or efficiency of the inverter can be challenging. However, radiated emissions are more likely to be a problem at higher frequencies (e.g. >30 MHz). One method for reducing common-mode current emissions at high frequencies is through the use of common-mode or differential-mode filters. Common-mode filtering can add significantly to the cost and weight of an inverter. Effective high-frequency differential-mode filtering can be difficult to implement without impacting the inverter performance, and imbalances in differential-mode filters can actually increase common-mode currents. This paper introduces the concept of a *balancing network* to reduce the common-mode currents on power inverter cables above 30 MHz. Balancing networks are relatively inexpensive to implement and can be more effective than common-mode chokes or ferrites. An experimental test set-up is used to demonstrate the effect of a balancing network on the common-mode current, differential-mode current and the common-mode rejection ratio on a balanced cable with an imbalanced termination. The results show that a balancing network reduces the common-mode noise currents significantly more than the differential-mode signal currents. This balancing network is also evaluated using a 3-phase brushless DC motor driver to verify its effectiveness in a real application.

## 1. Introduction

Power inverters convert electrical power at one voltage or frequency to power at another voltage or frequency. Most inverters employ pulse-width modulation schemes that rely on frequently switching signals with ultra-fast rise and fall times. These signals have significant energy at frequencies well above the fundamental switching frequency. Imbalances in the switching circuitry, transmission path, and load convert some of the power in the differential drive currents into common-mode noise currents (Fig. 1). These common-mode currents can interfere with other electronic devices, especially devices that rely on wireless communications.

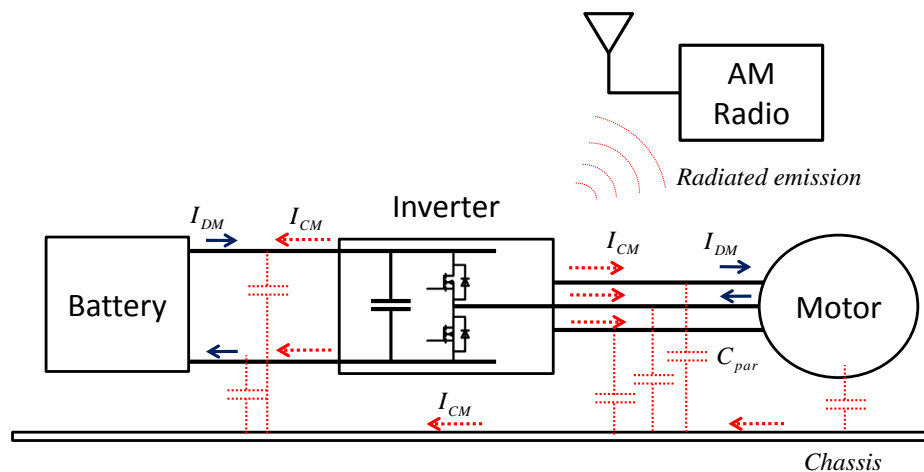


Fig. 1. Illustration of a typical power electronics system.

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A typical method of dealing with this form of electromagnetic interference is to apply common-mode filtering. However, this can add significantly to the cost and weight of a motor driver or power inverter and contributes nothing to the system's overall functionality or efficiency. A better approach is to actively enforce the electrical balance of the driver circuitry, while simultaneously compensating for imbalances in the transmission lines and load. Electrical balance is a measure of the relative impedance of the conductors in a circuit or transmission line to a zero-potential reference (ground) [1-4]. Changes in electrical balance convert differential-mode signals to common-mode noise. By ensuring that all of the signal or power-carrying conductors in a source-transmission-line-load configuration have the same impedance to ground, differential-to-common-mode conversion can be essentially eliminated.

Active balancing (i.e. actively compensating for naturally occurring changes in balance) at the operating frequency of power inverters has the potential to drastically reduce electrical noise and to actually improve the overall efficiency of the power transfer. However, actively compensating for changes in balance at frequencies as high as 30 MHz is generally not achievable. At high frequencies, passive balancing can be used to prevent the conversion of differential-mode signals to common-mode noise on cables.

This paper introduces the concept of a passive balancing network and demonstrates how passive balancing can be a cost-effective way to reduce common-mode currents on cables. An experimental test set-up is used to demonstrate the effect that a balancing network has on the common-mode (CM) current, differential-mode (DM) current and common-mode rejection ratio (CMRR) of a balanced cable with an imbalanced termination. Also, experimental results are compared to simulations based on full-wave modeling. A passive balancing network is then applied to a three-phase brushless direct current (BLDC) motor to verify its effectiveness in a real application.

## 2. Passive Balancing Networks

### 2.1 Electrical Balance

Several models have been introduced to describe differential-mode to common-mode conversion. Hockanson [5] introduced current-driven and voltage-driven source models to describe how differential-mode signals on circuit boards induce common-mode currents on attached wires.

An equivalent model for estimating the radiated emissions from a printed circuit board with attached cables driven by a signal voltage on a trace was developed by Shim [6]. This model employed a common-mode voltage source located at the junction between the PCB ground structure and the attached wire. The magnitude of common-mode voltage was proportional to the ratio of the self-capacitance of the trace to that of the return plane of a PCB structure.

Watanabe [1] introduced the concept of a *current division factor* to quantify the electrical imbalance of various transmission line configurations. He showed that imbalance is not responsible for the conversion of differential-mode currents to common-mode currents. This conversion is the result of *changes* in the level of imbalance. Using various printed circuit board structures as examples, he showed that it is possible to calculate the common-mode currents by replacing the differential-mode source with equivalent common-mode sources at points where changes in the imbalance occur. This imbalance difference modeling technique can greatly simplify the analysis of radiated emissions due to common-mode currents.

Several factors contribute to imbalance in power inverter systems: geometrical asymmetries, unequal turn-on and turn-off times of the switching components, unbalanced PWM control schemes, unbalanced filtering, switching device parasitics, and imbalances in the load impedance. These sources

of imbalance can convert the rapidly switching differential-mode currents to common-mode currents resulting in EMI problems [7].

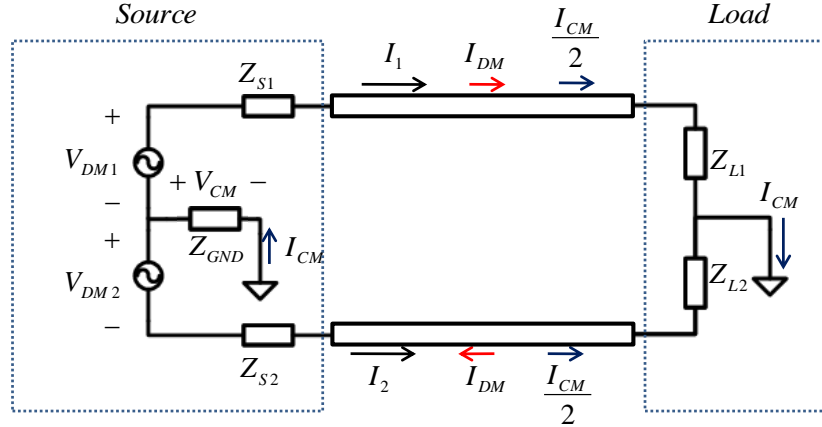


Fig. 2. Circuit with DM and CM currents.

Fig. 2 shows a circuit with DM and CM currents. This circuit has dual differential-mode voltage sources, a single common-mode source impedance connected to ground, differential source and load impedances, and a transmission path as shown. If the two wires connecting the source to the load have the same impedance to ground, the currents  $I_1$  and  $I_2$  flowing on the two wires can be decomposed into two modes,  $I_{DM}$  and  $I_{CM}$ , defined as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 1/2 & 1 \\ 1/2 & -1 \end{bmatrix} \begin{bmatrix} I_{CM} \\ I_{DM} \end{bmatrix}. \quad (1)$$

The differential-mode current,  $I_{DM}$ , and the common-mode current,  $I_{CM}$ , on these balanced wires can be determined from  $I_1$  and  $I_2$  as

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1/2 & -1/2 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (2)$$

## 2.2 Imbalance factor

Watanabe et al. [1, 2] developed techniques for quantitatively defining electrical imbalance and developed a method for calculating common-mode currents using equivalent common-mode voltage sources. Watanabe showed that the common-mode current in a system can be precisely modeled by placing an equivalent common-mode voltage source in the circuit at places where changes in the imbalance occur. The amplitude of these voltage sources is given by

$$\Delta V_C = \Delta h \times V_{DM} \quad (3)$$

where  $\Delta h$  is the change in the current division factor (or *imbalance factor*) and  $V_{DM}$  is the differential-mode voltage at that point in the circuit.

Fig. 3 illustrates how this approach is applied. Fig. 3(a) shows a pair of cable conductors above a ground plane with the source and load impedances indicated. In Fig. 3(b), if we assume that  $V_{DM1} = -V_{DM2}$ ,  $Z_{S1} = Z_{S2}$ , and  $Z_{Cable1-gnd} = Z_{Cable2-gnd}$ , then Part A of the circuit is perfectly balanced ( $h_A = 0.5$ ). Part B of the circuit has an imbalance factor,

$$h_B = \frac{Z_{L2}}{Z_{L1} + Z_{L2}} = \frac{Y_{L1}}{Y_{L1} + Y_{L2}} = \frac{I_{CM1}}{I_{CM1} + I_{CM2}}. \quad (4)$$

The equivalent source that drives the common-mode current is then given by

$$\Delta V_C = |h_B - h_A| \times V_{DM_{Load}} = \left| \frac{Z_{L2}}{Z_{L1} + Z_{L2}} - 0.5 \right| \times V_{DM_{Load}} \quad (5)$$

where  $V_{DM_{Load}}$  is differential-mode voltage across the load. The common-mode currents in the imbalance difference model (Fig. 3(b)) are exactly equal to the common-mode currents in the original circuit, Fig 3(a). Note that if  $Z_{L1} = Z_{L2}$  in (5), the equivalent common-mode voltage and the common-mode currents are zero.

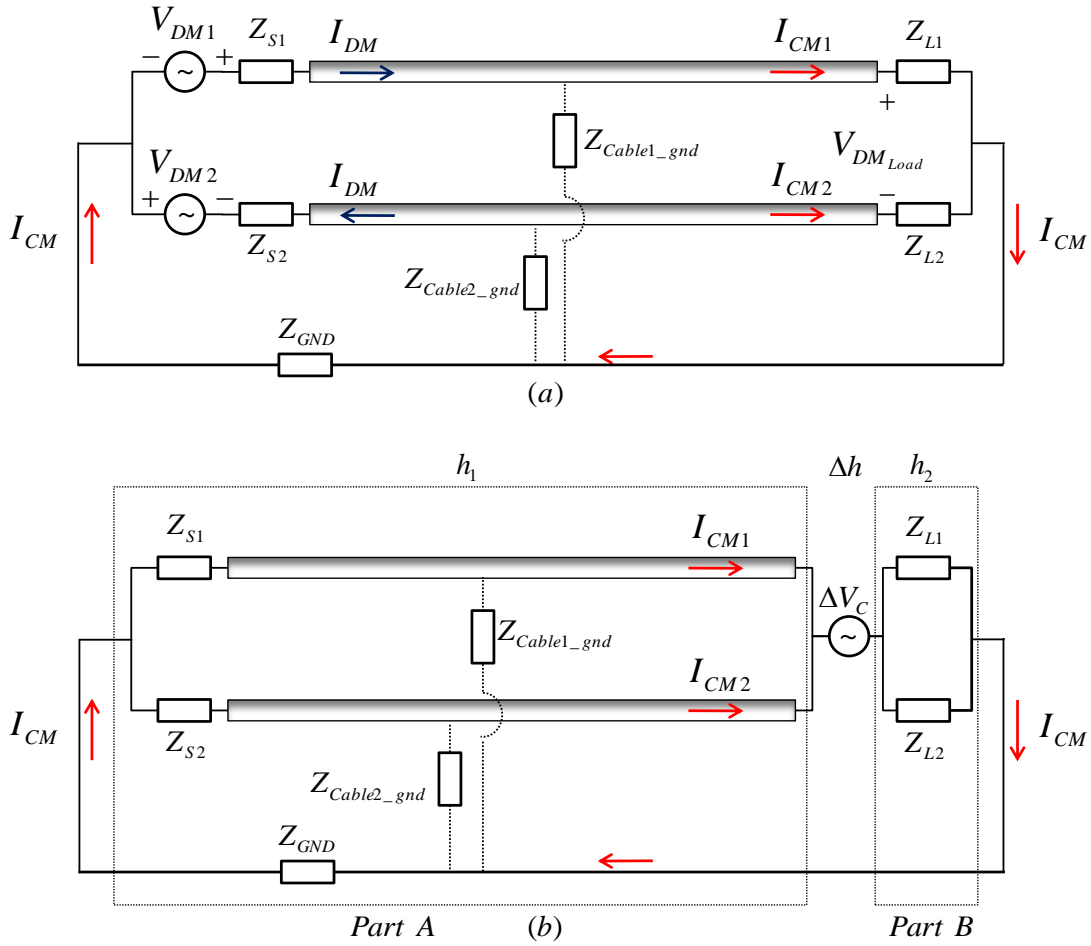


Fig. 3. Common-mode currents generated from unbalanced load condition (a) and imbalance difference model (b).

There is no common-mode current if both parts of the circuit are balanced. There is also no common-mode current if both parts are equally unbalanced. In unbalanced circuits, it is necessary to define the relationship between  $I_1$ ,  $I_2$ ,  $I_{CM}$  and  $I_{DM}$  as [1],

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h & 1 \\ 1-h & -1 \end{bmatrix} \begin{bmatrix} I_{CM} \\ I_{DM} \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1-h & -h \\ 1 & 1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \quad (7)$$

In balanced circuits ( $h = 0.5$ ), (6) and (7) are the same as (1) and (2), respectively. Whether the circuit is balanced or unbalanced, the common-mode current,  $I_{CM}$ , is the sum of the currents on both wires.

### 2.3 Balancing Networks

Common-mode current on balanced cables can be reduced by introducing *balancing networks* to compensate for imbalances in the source or load as illustrated in Fig. 4. These balancing networks, indicated by the components with a BN subscript in Fig. 4, are designed to have an impedance that is lower than the existing source and load impedances at the frequencies where they are effective.

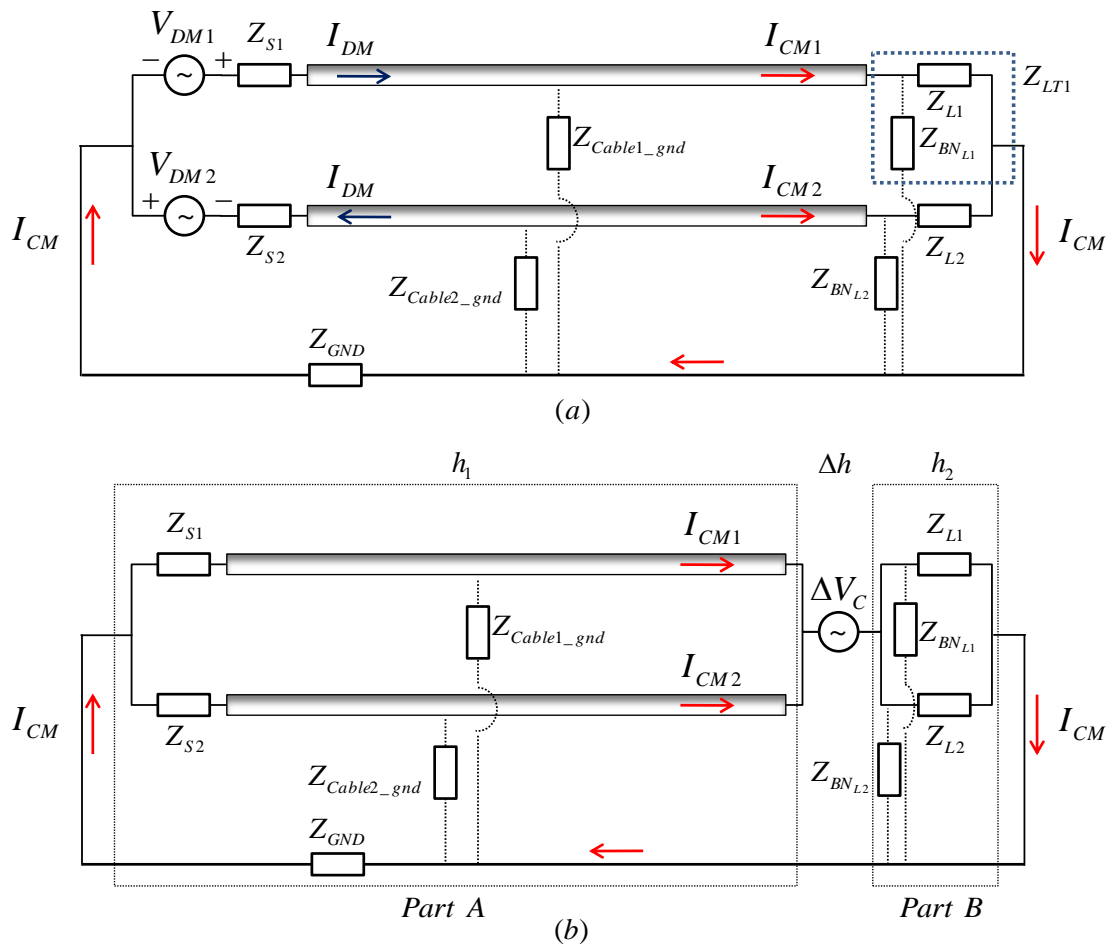


Fig. 4. Equivalent circuit of wire model with balancing network (a) and its imbalance difference model (b).

The precise value of the impedance is not critical, but it is important that the impedances on each side of the circuit are the same. The goal of the balancing network is to make the impedance of each phase have the same value as viewed from the cable looking into the source and load.

If our goal is to balance the circuit at high frequencies without affecting the operation of the circuit at low frequencies, a good choice for a balancing network is a resistor,  $R_B$ , in series with a capacitor,  $C_B$ . This circuit has a high impedance and is relatively invisible at low frequencies. At high frequencies

it has an impedance equal to its resistance, which is relatively stable and easy to match to other resistances in the balancing network.

In this paper,  $Z_{BN}$  is a series RC ( $R_B$ ,  $C_B$ ) circuit connecting each phase wire to system ground. In the circuit in Fig. 4(a), the impedance looking into the load from each phase wire (including the RC balancing network),  $Z_{LT}$ , is

$$Z_{LT1} = Z_{L1} // Z_{BN_{L1}} = 1 / \left( \frac{1}{Z_{L1}} + \frac{1}{Z_{BN_{L1}}} \right) = \frac{Z_{L1} \times Z_{BN_{L1}}}{Z_{L1} + Z_{BN_{L1}}} = \frac{Z_{L1} \times (j\omega R_{B1} C_{B1} + 1)}{j\omega R_{B1} C_{B1} + 1 + j\omega Z_{L1} C_{B1}}, \quad (8-1)$$

$$Z_{LT2} = Z_{L2} // Z_{BN_{L2}} = 1 / \left( \frac{1}{Z_{L2}} + \frac{1}{Z_{BN_{L2}}} \right) = \frac{Z_{L2} \times Z_{BN_{L2}}}{Z_{L2} + Z_{BN_{L2}}} = \frac{Z_{L2} \times (j\omega R_{B2} C_{B2} + 1)}{j\omega R_{B2} C_{B2} + 1 + j\omega Z_{L2} C_{B2}}. \quad (8-2)$$

Fig. 5 shows how the RC balancing network causes the load impedance to ground of each phase wire to approach the same value at high frequencies without affecting the low-frequency differential load impedance. For this calculation, the load impedances without the balancing network are,  $Z_{L1} = 178 \Omega$  and  $Z_{L2} = 90 \Omega$ . The RC balancing network component values are  $R_B = 51 \Omega$  and  $C_B = 1$  nF. As shown in Fig. 5, near balance is achieved at frequencies above approximately 20 MHz.

Although the balance is not perfect ( $h_{with\_BN} = \frac{51 // 90}{(51 // 90) + (51 // 178)} = 0.45$ ), it is significantly improved

relative to its value at low frequencies ( $h_{without\_BN} = \frac{90}{90 + 178} = 0.33$ ). The equivalent common-mode voltage is proportional to the change in the balance factor, so the reduction in common-mode voltage with this balancing network at high frequencies would be,

$$20 \log \frac{h_{cable} - h_{without\_BN}}{h_{cable} - h_{with\_BN}} = 20 \log \frac{0.50 - 0.33}{0.50 - 0.45} = 10.6 \text{ dB}. \quad (9)$$

Fig. 6 shows the actual common-mode current calculated for the circuit in Figs. 3 and 4, without and with the balancing network. The balancing network and load impedances used for this calculation were the same as in Fig. 4. The source impedances were  $Z_{S1} = Z_{S2} = 75 \Omega$ . The source voltages were  $V_{DM1} = -V_{DM2} = 0.5$  V.  $Z_{GND}$  was zero.



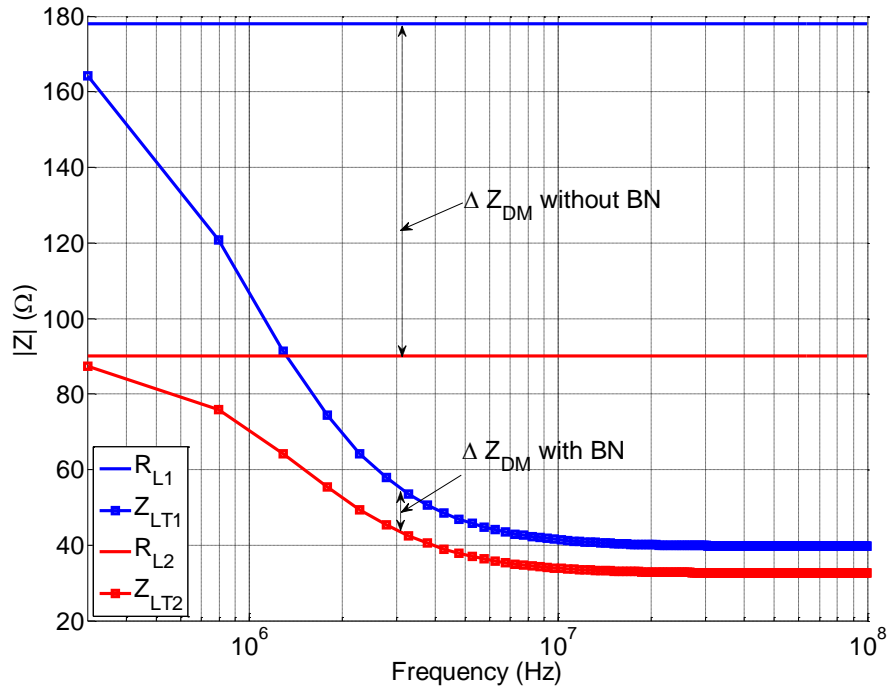


Fig. 5. Imbalance at ‘without’ and ‘with’ balancing network (BN).

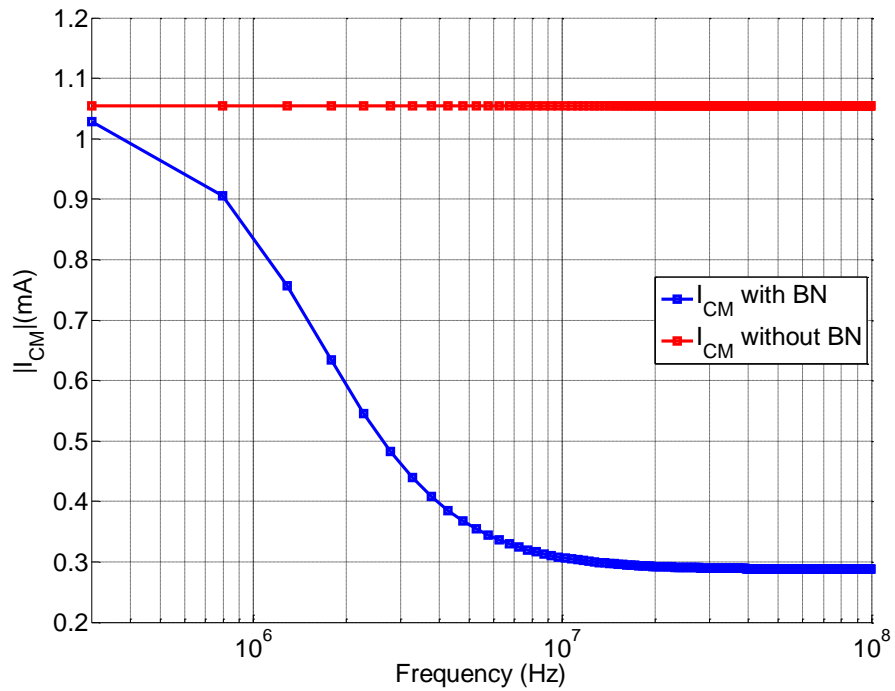


Fig. 6.  $I_{CM}$  comparison depending on the balancing network at load side.

### 3. Evaluation of a HF Balancing Network

The test set-up illustrated in Fig. 7(b), was used to demonstrate how a balancing network can reduce common-mode currents. The equivalent circuit for this set-up, Fig. 7(a), has two voltage sources with opposing polarities,  $V_{DM1}$  and  $V_{DM2}$ , that drive a pair of wires above a ground plane. The normalized amplitude of  $V_{DM}$  is 1.0 V. Each wire is terminated with a resistor to the ground plane. To create an unbalanced condition, the load resistors were given different values,  $Z_{L1} = 178.3 \Omega$  and  $Z_{L2} = 91 \Omega$ . The total differential-mode termination impedance is  $Z_{L1} + Z_{L2} = 269.3 \Omega$ . The length of the wires between the source and load is 920 mm.

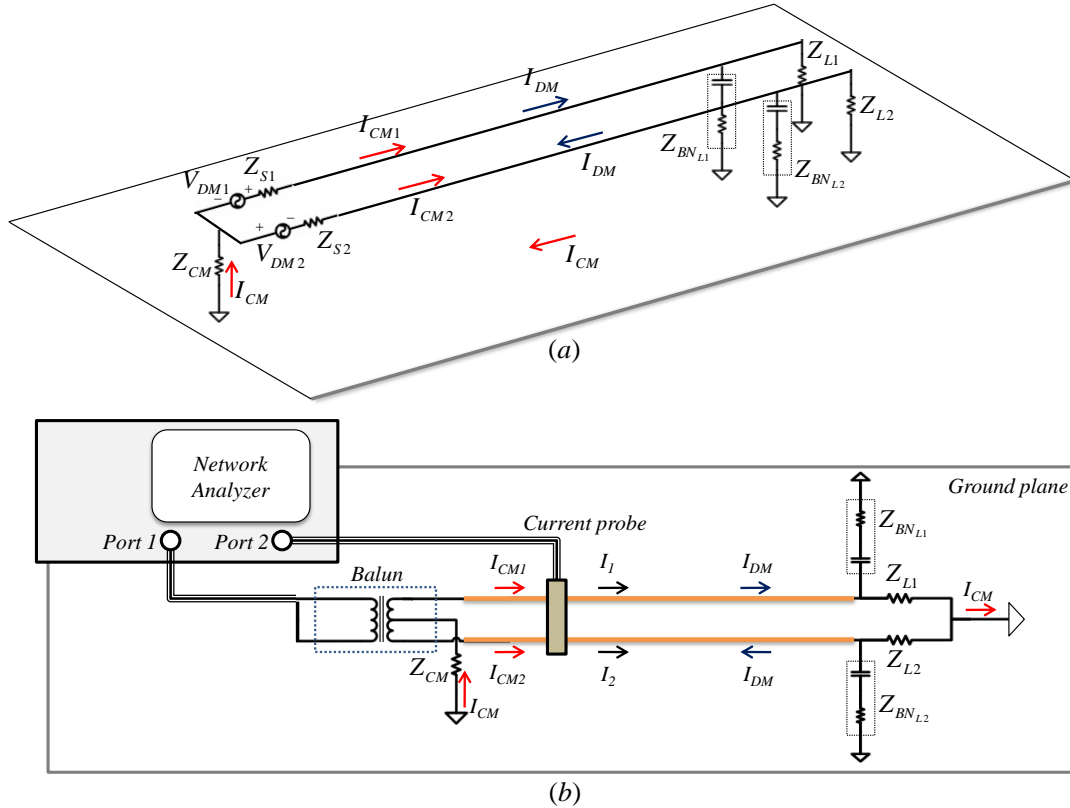


Fig. 7. Equivalent circuit (a) and test configuration (b) used to demonstrate the balancing effect.

The magnitude of the transfer coefficient,  $|S_{21}|$ , between port 1 and port 2 of the network analyzer was measured to determine the relationship between the common-mode (CM) current and differential mode (DM) current in the circuit. Port 1 of the network analyzer was connected to the single-ended side of a wide-band transformer (balun). Port 2 was connected to a current probe (FCC F-33-1), which was clamped around both wires to measure the common-mode current. To measure the differential-mode current, current probes were placed around each of the wires. While measuring the differential-mode current,  $I_1$  or  $I_2$ , both current clamps were in place in order to avoid any unbalancing of the circuit due to current clamp loading. An Agilent E5070B Network Analyzer was used to measure  $S_{21}$  from 1 MHz to 100 MHz.

The balancing network is indicated by the series R-C circuits labeled  $Z_{BNL1}$  and  $Z_{BNL2}$  in Fig. 7. The value of each capacitor in the balancing network is  $0.001 \mu\text{F}$ , and each resistor is  $51 \Omega$ . This RC combination has little effect on the termination impedance below  $f_c = 1/2\pi RC = 3 \text{ MHz}$ . At 30 MHz and higher, its nominal impedance is approximately  $51 \Omega$ .

### 3.1 Correlation of the $|S_{21}|$ measurement with current amplitude

For the configuration in Fig. 7, the value of  $|S_{21}|$  is a measure of the ratio of the common-mode current,  $I_{CM}$ , to the differential-mode voltage at the output of the balun,

$$20\log_{10}|S_{c1}| = 20\log_{10}\left|\frac{I_{CM} \times 50}{V_{DM}}\right| + \text{Calibration\_Factor}(dB) \quad (10)$$

where  $\text{Calibration\_Factor}(dB)$  is a constant determined by the transfer coefficients of the balun, current probes, and other fixed pieces of the test set-up. If we assume that the differential-mode current is much greater than the common-mode current, and the current probe on Port 2 is clamped around just one wire,  $|S_{21}|$  is a measure of the ratio of the differential-mode current,  $I_{DM}$ , to the differential-mode voltage at the balun,

$$20\log_{10}|S_{d1}| = 20\log_{10}\left|\frac{I_{DM} \times 50}{V_{DM}}\right| + \text{Calibration\_Factor}(dB). \quad (11)$$

A common-mode rejection ratio (CMRR) can be defined as the ratio of the differential-mode current to the common-mode current. Higher values indicate better rejection of the common mode. The CMRR for the configuration in Fig. 7 is given by the difference (in dB) between measurements of  $|S_{21}|$  with the current clamp around one wire and both wires,

$$\text{CMRR (dB)} = 20\log_{10}\left|\frac{I_{DM}}{I_{CM}}\right| = 20\log_{10}|S_{d1}| - 20\log_{10}|S_{c1}| \quad (12)$$

### 3.2 Characteristic impedance of coupled transmission line

In Fig. 8, the height from ground to the center of the each wire,  $height$ , is 35 mm, the distance between the two wires,  $d$ , is 25 mm, and the radius of the wire,  $r$ , is 2.5 mm. The width of the plane in this test set-up,  $w$ , is 230 mm.

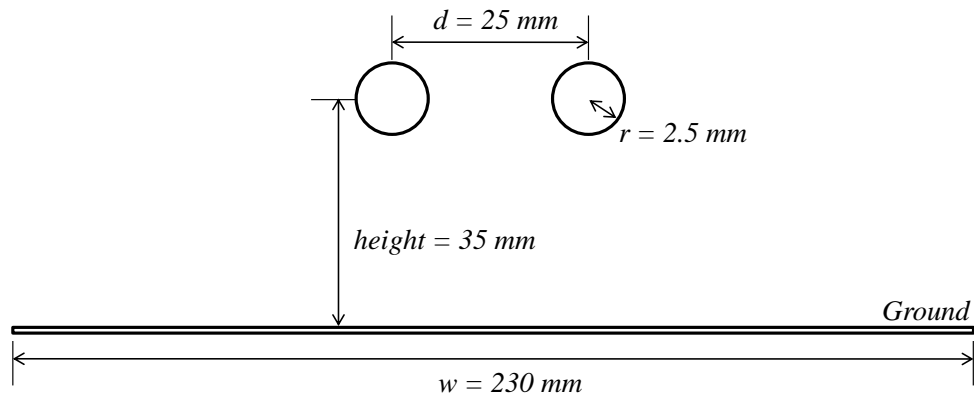


Fig. 8. Cross-sectional geometry of test configuration.

Using a two-dimensional static electric-field simulation tool [39], it was determined that  $Z_{11}$  (equal to  $Z_{22}$ ) and  $Z_{12}$  (equal to  $Z_{21}$ ) were  $201.9 \Omega$  and  $67.4 \Omega$ , respectively, and the differential-mode characteristic impedance  $Z_{DM}$  was  $269.3 \Omega$ . In this configuration, the load impedances ( $Z_{L1} = 178.3 \Omega$ ,  $Z_{L2} = 91 \Omega$ ) without the balancing network provide a matched termination for the differential-mode signals.

### 3.3 Balun characteristics

In order to correlate model results with measurement results, the CM and DM impedances of the balun had to be determined. As illustrated Fig. 9, a 50-Ω load was used to terminate the input side of the balun, while measuring the impedance looking into the balun output. The DM impedance was the impedance between the two output pins of the balun as indicated in the upper part of Fig. 9. The CM impedance was the impedance measured between the two output pins tied together and the grounded center-tap of the balun output as indicated in the lower part of the figure. The measured balun impedances are plotted in Fig. 10.

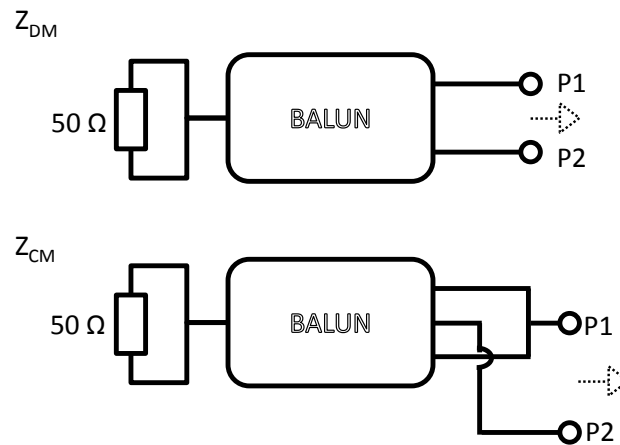


Fig. 9. Test configuration to measure  $Z_{CM}$  and  $Z_{DM}$  of the balun output.

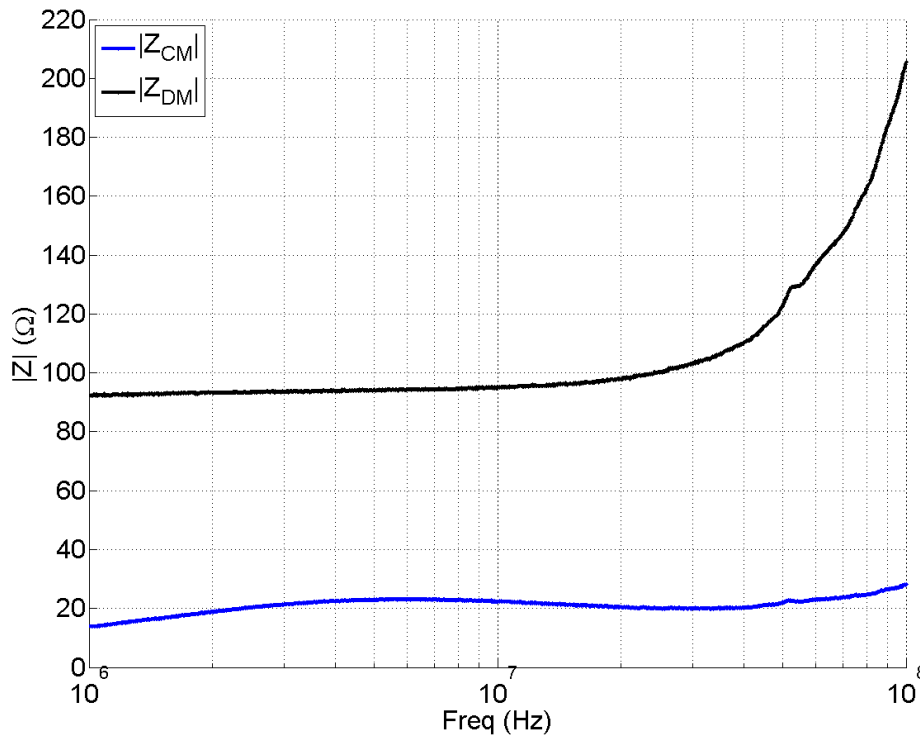


Fig. 10. Measured values of the balun's CM and DM impedance.

The common-mode impedance of the coupled transmission line in Fig. 8 is  $67 \Omega$ , while the CM impedance of the balun is approximately  $20 \Omega$ . Thus, a  $46.5\text{-}\Omega$  resistor was added between the center tap of balun and the ground plane to help match the common mode. The impedances,  $Z_{S1}$  and  $Z_{S2}$  in Fig. 7 each represent half of the balun's DM output impedance, which is a function of frequency as indicated in Fig. 10. The measured balun impedances used for modeling this test configuration are listed in Table I.

Table I. Measured values of  $Z_{CM}$  and  $Z_{DM}$  for the balun

Frequency	$Z_{CM}$	$Z_{DM}$	$Z_{CM}+46.5\Omega$	$Z_{DM}/2 (= Z_{s1} = Z_{s2})$
1 MHz	13.8	92.3	60.3	46.2
2 MHz	18.9	93.2	65.4	46.6
3 MHz	21.3	93.6	67.8	46.9
4 MHz	22.3	93.6	68.8	46.9
5 MHz	23.0	94.3	69.5	47.2
6 MHz	23.0	94.1	69.5	47.0
7 MHz	23.0	94.5	69.5	47.0
8 MHz	22.9	94.5	69.4	47.1
9 MHz	22.7	95.2	69.1	47.6
10 MHz	22.4	94.9	68.8	47.5
20 MHz	20.6	97.9	67.0	48.9
30 MHz	19.9	103.2	66.4	51.6
40 MHz	20.3	110.4	66.7	55.2
50 MHz	22.2	123.1	68.7	61.6
60 MHz	23.0	136.6	69.5	68.3
70 MHz	23.6	147.2	70.1	73.6
80 MHz	24.7	162.4	71.3	81.2
90 MHz	26.5	183.8	72.9	91.9
100 MHz	28.1	205.5	74.6	102.7

### 3.4 Full-wave modeling

A full-wave analysis (using FEKO [40]) was applied to the configuration in Fig. 7. The essential elements of the model are illustrated schematically in Fig. 11 with and without the balancing network in place. In these models, the 92-cm wire length was divided into 100 segments.  $V_{DM1}$  and  $V_{DM2}$  were set to 1 V.  $Z_{S1}$ ,  $Z_{S2}$  and  $Z_{CM}$  were given the frequency-dependent values indicated in Table I.  $Z_{L1}$  was  $178.3 \Omega$  and  $Z_{L2}$  was  $91 \Omega$ . The currents  $I_1$  and  $I_2$  were monitored at the 1<sup>st</sup> segment to find  $I_{CMS}$  and  $I_{DMS}$  at the source side, and at the 100<sup>th</sup> segment to determine  $I_{CML}$  and  $I_{DML}$  at the load side.

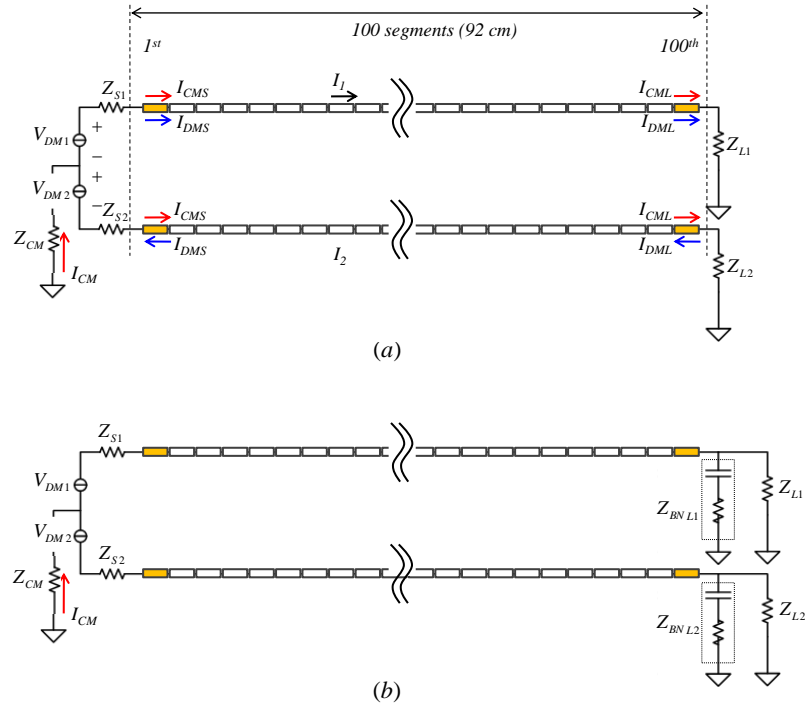


Fig. 11. Wire segmentation and termination for modeling without BN (a) and with BN (b).

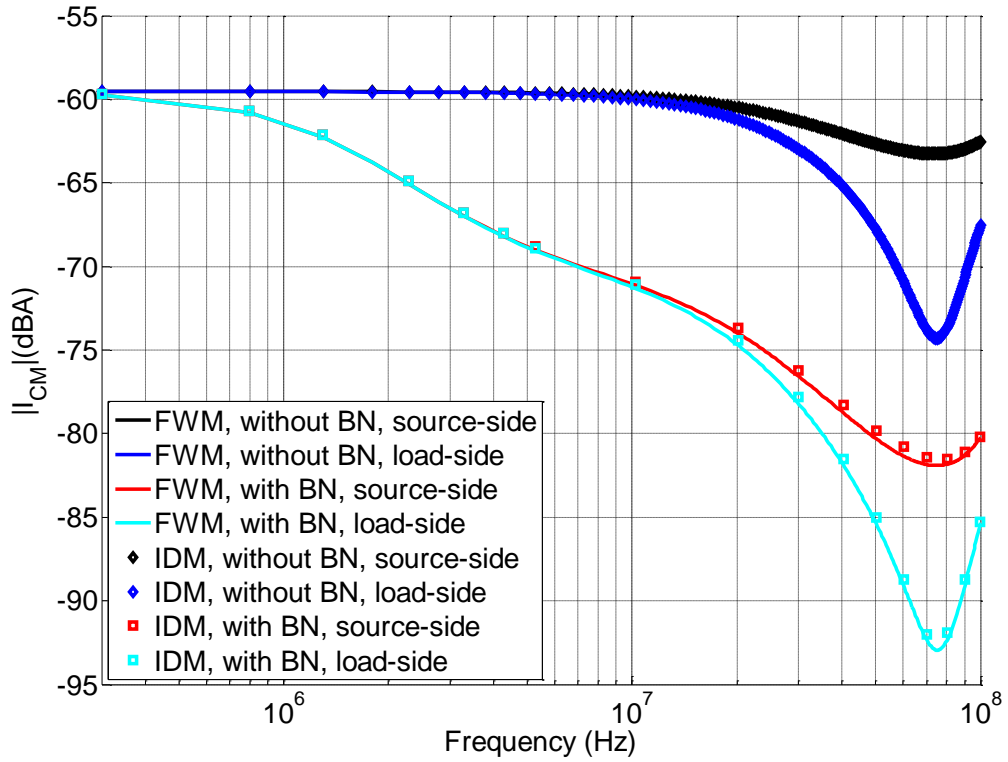


Fig. 12.  $I_{CM}$  comparison with BN and without BN.

### 3.5 Comparison with imbalance difference model (IMD)

Fig. 12 shows the magnitude of the common-mode current in the Fig. 7 test set-up as calculated using the full-wave model and the imbalance difference model with the imbalance parameters in Equation (9). Both analyses are well correlated between 300 kHz and 100 MHz. Because there was no need to model the balun for this comparison, the 46.5- $\Omega$  resistor for common-mode impedance matching at the source side was left out of the circuit and the differential-mode impedance value of the source side was fixed to 150  $\Omega$  instead of the frequency-dependent value in Table I.

### 3.6 Measurement results

The balancing network should not have a significant effect on the differential-mode current below the 3-MHz cutoff frequency. Fig. 13 shows the measured  $|S_{21}|$  (proportional to  $I_{DM}$ ) with and without the balancing network in place. At 10 MHz, the balancing network increases the current at the load end of the circuit by 6 dB. At approximately 80 MHz, where the wires are a quarter-wavelength long, the effect on the current is greater. This is because the balancing network creates a mismatch between the differential-mode characteristic impedance of the transmission line and the differential-mode termination impedance.

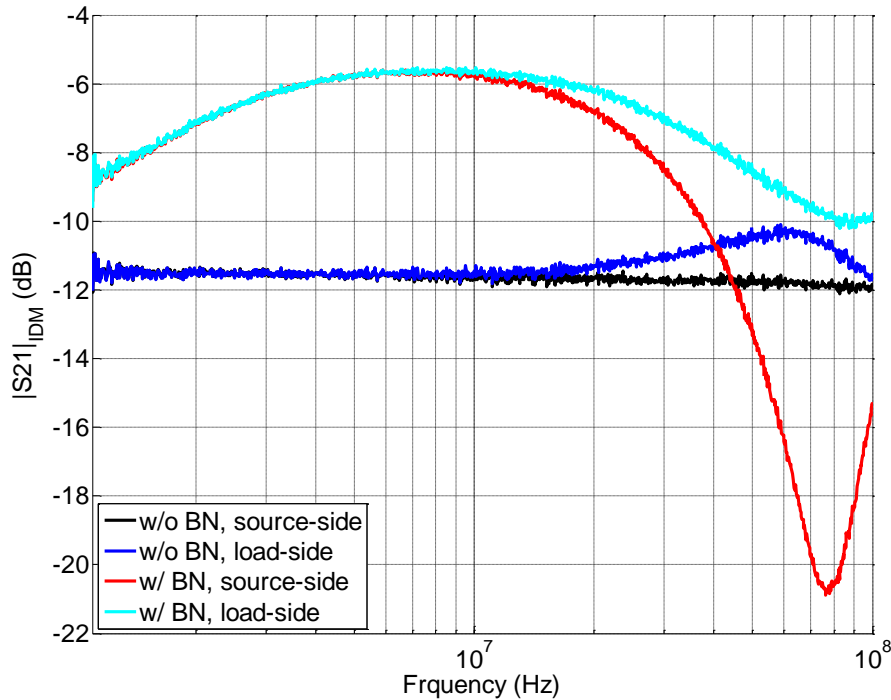


Fig. 13.  $I_{DM}$  response depending on the different monitoring locations.

Fig. 14 shows the measured  $|S_{c1}|$  (proportional to  $I_{CM}$ ) with and without the balancing network. The balancing network attenuates the common-mode current by about 7.5 dB at 3 MHz, and the attenuation is 15 dB or more between 30 and 100 MHz.

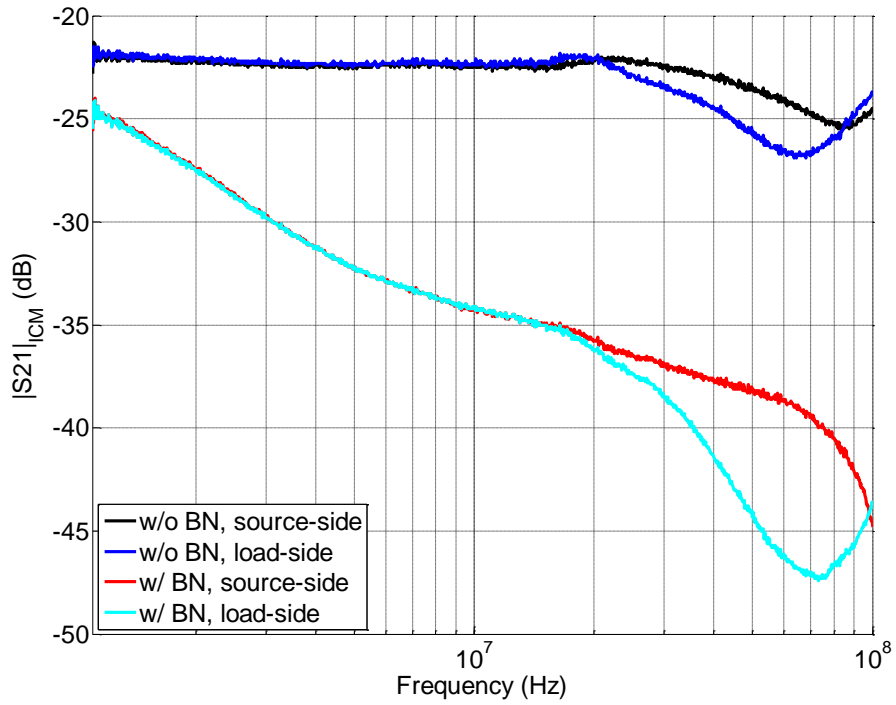


Fig. 14.  $I_{CM}$  response depending on the different monitoring locations.

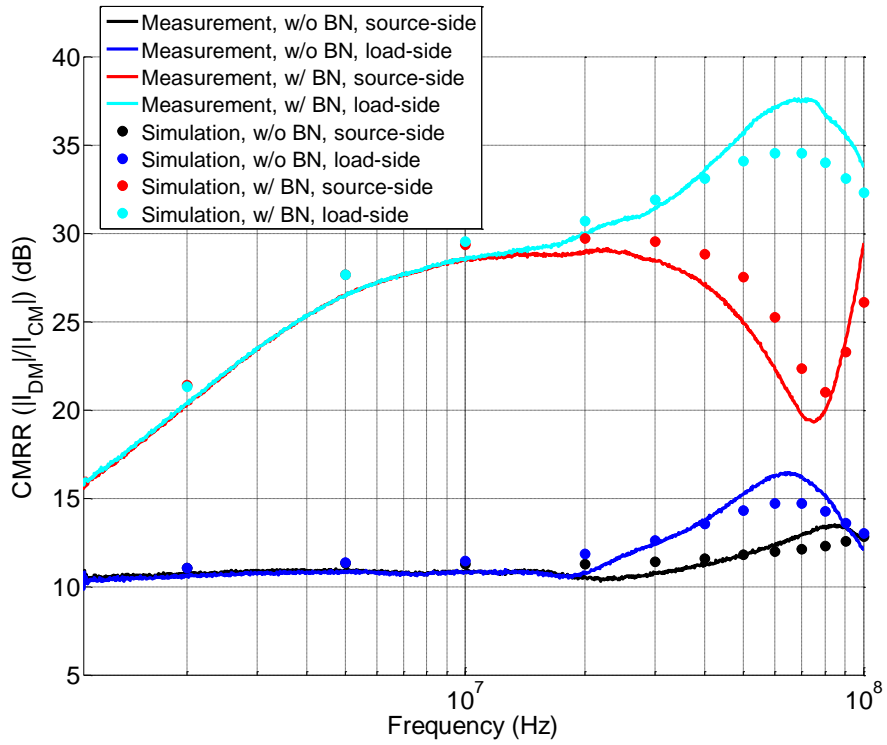


Fig. 15. Measured and simulated CMRR ( $|I_{DM}/I_{CM}|$  in dB).

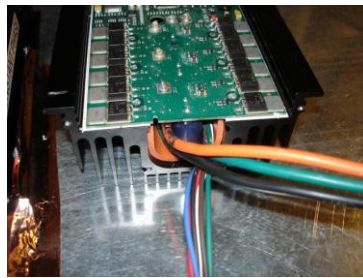


Fig. 15 shows the CMRR with and without the balancing network. Both measured results and full-wave simulation results are shown. With the balancing network in place, the CMRR is more than 30 dB higher between 30 and 70 MHz on the load side. On the source side, where the differential-mode currents experience a null around 80 MHz, the CMRR is still improved by at least 6 dB with the balancing network in place.

Note that in this measurement, the balancing network increases the mismatch between the characteristic impedance of the transmission line and the differential-mode termination impedance. These values were chosen to make the point that the reduction in common-mode current had nothing to do with better matching. In practical applications, the resistances of the balancing network could be chosen to improve the matching of the differential-mode signal, rather than make it worse.

#### 4. A Power Inverter Application

The fast switching that is an inherent part of efficient motor drives and power inverters produces a high amount of electrical noise. Imbalances in the switching circuitry, transmission path, and load convert differential drive noise into common-mode currents that can be significant sources of broadband radiated emissions typically peaking around 30 - 70 MHz. These emissions can interfere with other electronic devices, especially devices that rely on wireless communications. The 3-phase inverter and brushless direct-current (BLDC) motor illustrated in Fig. 16 exhibited unacceptable levels of radiated emissions at frequencies between 30 and 70 MHz. These emissions were due to the common-mode current flowing on the cable connecting the inverter to the motor.



(a)



(b)

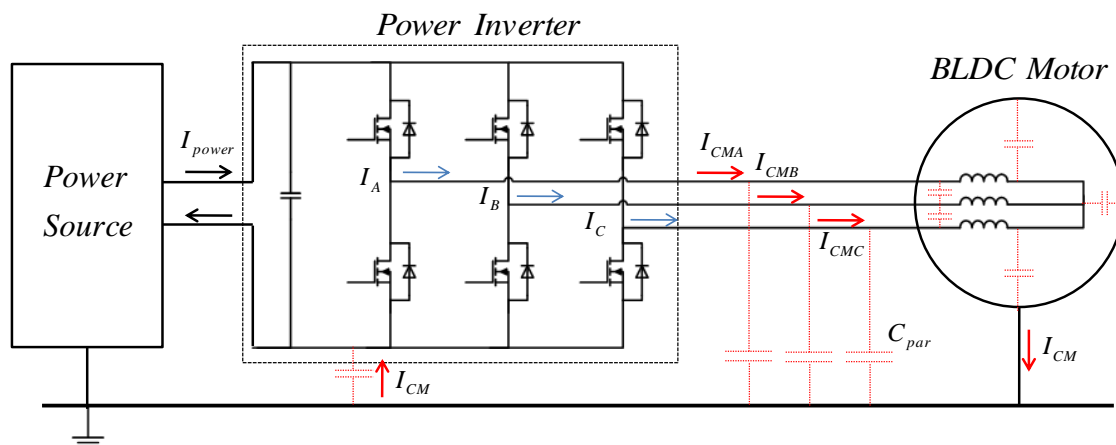


Fig. 16. Three-phase BLDC Motor system; (a) power inverter (b) BLDC motor.

The objective of the balancing network is to provide a constant, balanced impedance to the transmission lines between the inverter and the BLDC motor at frequencies between 30 and 70 MHz. A 1-nF capacitor in series with a 51-ohm resistor was connected between each phase wire and a local ground plane at each end of the cable as shown in Fig. 17. This provided a constant impedance of approximately 50 ohms from each wire to the ground plane of the balancing network. 50 ohms was chosen as a value that was low relative to the inverter output impedance and motor input impedance at 30 MHz, but high enough to overwhelm the impedance associated with the inductance of the connection between the components and the ground plane. While it is important that all three terminations have the same impedance to ground, the exact value of this impedance is not critical.

The cable length between power inverter and BLDC motor was about 1.5 m and the test configuration was set up on a metal table top that connected to the chassis ground of the inverter and the wires lied on a 7-mm thick insulating pad.

The common-mode current was measured using a current probe connected to a spectrum analyzer. In these tests, the BLDC motor was loaded by driving another motor through a shaft.

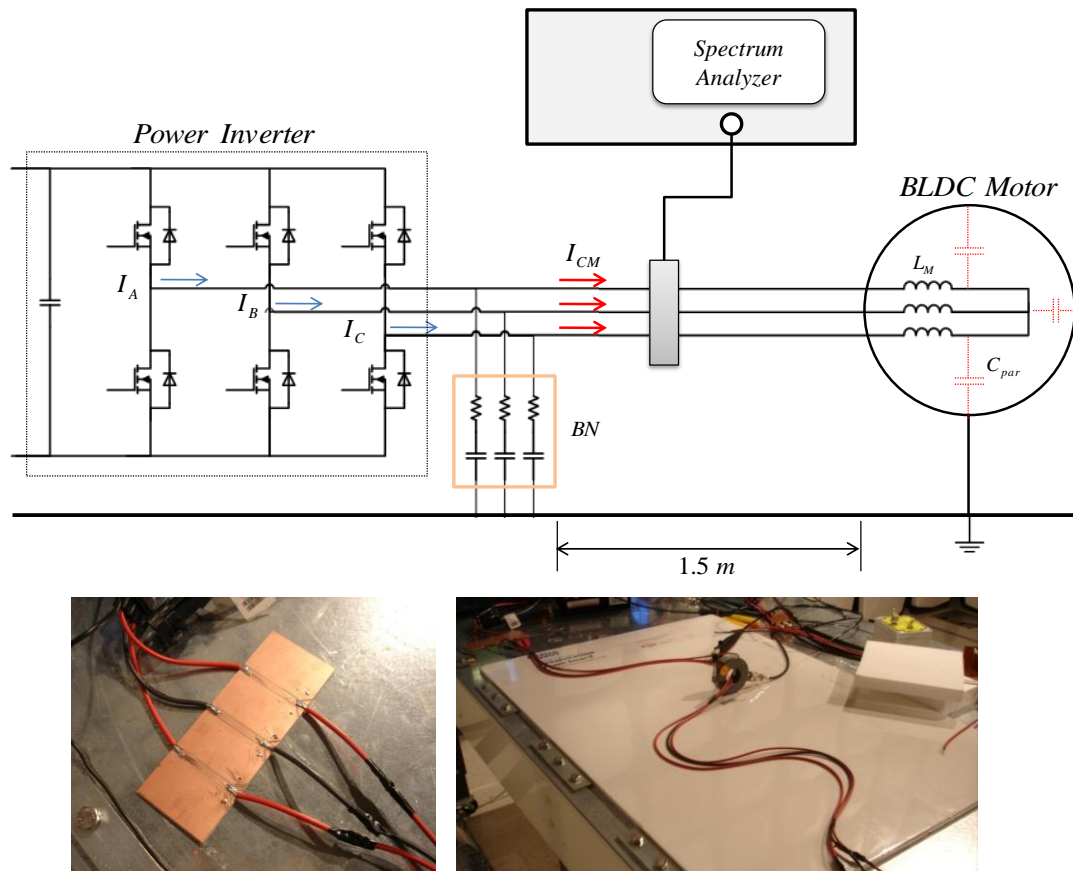


Fig. 17. Test configuration for evaluating the balancing network.

A three-phase motor/driver system like this would be perfectly balanced if the impedance of all three phase wires to ground was the same, and if the average of the voltages between each wire and ground were constant. In a balanced system, there would be no conversion of differential-mode currents to common-mode currents. The six-step PWM driving scheme employed by this inverter system is inherently unbalanced. At various stages of the drive cycle one or two of the phase wires may be floating, tied high or tied low. Fig. 18 shows the measured phase voltage (to chassis ground), gate voltage on the high side MOSFET, and line current for one of the three wires in this system.

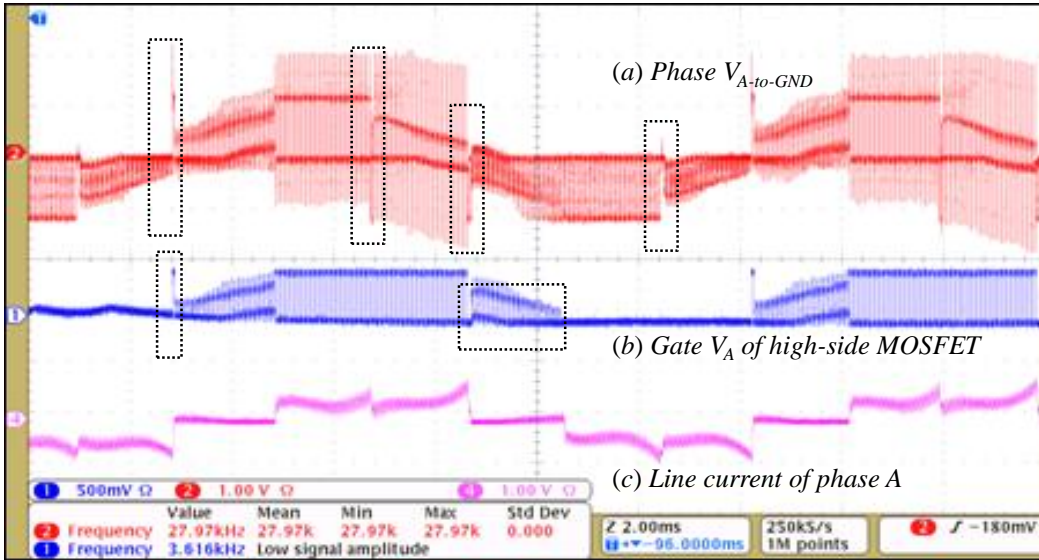


Fig. 18. Phase voltage and line current from one of three-phase cables.

Fig. 19 plots the common-mode current on the three wires without the balancing network. The upper plot is in the time domain and the lower plot shows the frequency components from 30 to 80 MHz as a function of time. Spikes in the common-mode current correlate with the spikes in the differential-mode current that occur during the switching of the MOSFETs. The original design suppressed these currents using ferrite cores clamped around the cable.

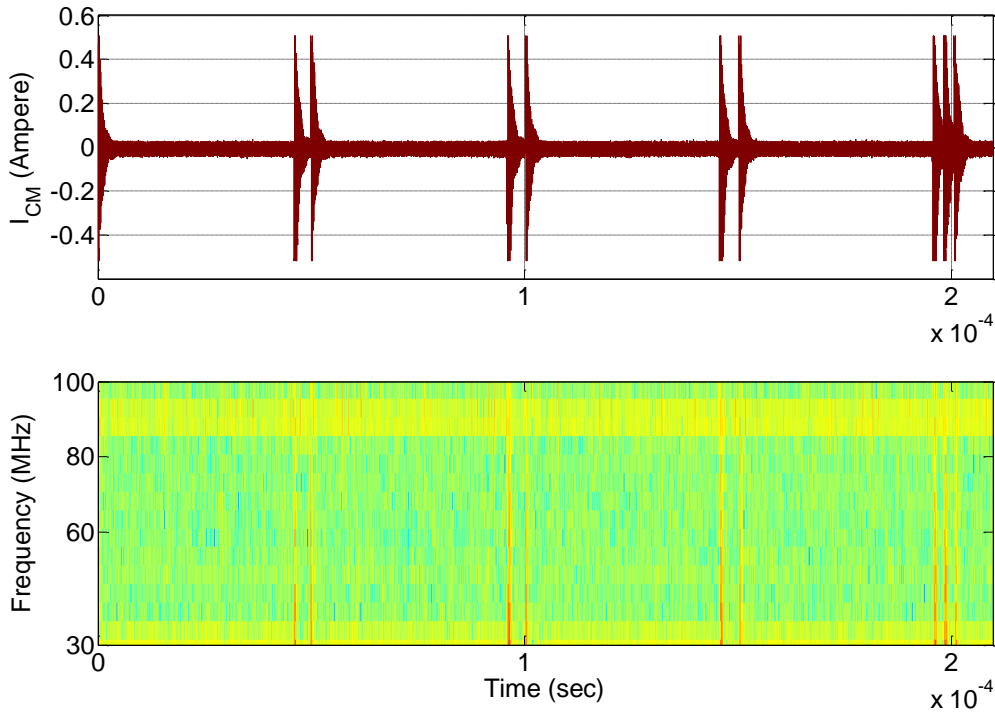


Fig. 19. Measured  $I_{CM}$  waveforms and short-term FFT.

The maximum common-mode current was observed when the inverter was driving the motor at maximum speed. The maxhold function of the spectrum analyzer was used to capture the maximum level of common-mode current on the 3-wire cable. The current supplied to the inverter was adjusted to 2.0 amperes. As shown in Fig. 20, when the balancing network was applied to the phase wires at the output side of the power inverter, the common-mode noise on the cable between 30 and 80 MHz was significantly reduced.

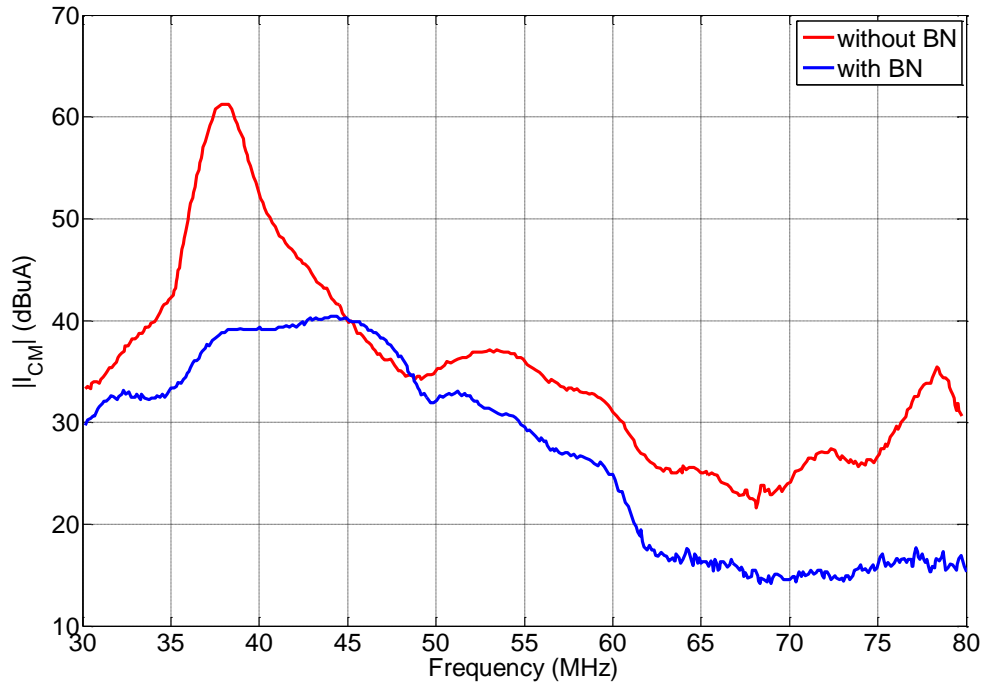


Fig. 20.  $I_{CM}$  at maximum speed.

## 5. Conclusion

Differential-mode voltages can be converted to common-mode currents by changes in circuit balance resulting in EMI problems. Passive balancing networks can cost-effectively prevent DM-to-CM conversion at high frequencies without impacting the low-frequency operation of the circuit. Unlike DM filtering, passive balancing has a greater effect on CM currents than it does on DM currents. Unlike most CM filtering, passive balancing networks can be highly effective without requiring relatively bulky and expensive inductors or ferrites. However, it should be noted that passive balancing networks only attenuate common-mode currents that result from changes in imbalance. They do not attenuate common-mode currents resulting directly from common-mode sources.

One particularly attractive application of passive balancing is the suppression of common-mode currents in power inverters. Power inverters rely on very fast switching at kHz frequencies. Since most power inverter driving schemes are inherently unbalanced, the differential-mode signals produced by these inverters can be converted to common-mode currents in balanced cables and loads. Filtering power inverter outputs can be expensive and/or affect the efficiency of the inverter. Balancing networks can significantly reduce the common-mode currents from power inverters without similarly attenuating the differential-mode drive currents.

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