CVEL

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Non-Linear Resistance of Multi-layer Ceramic Capacitors Caused by Electrostatic Discharge

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Table of Contents

Abstract

The paper investigates the susceptibility of multi-layer ceramic (MLC) capacitors to electrostatic discharge (ESD). For the capacitors investigated in this study with the same voltage rating and package size, the capacitors with lower capacitance were more susceptible to ESD. The degradation of MLC capacitors subjected to repeated discharges manifests itself as a non-linear resistance. The current leaking through the capacitor increases exponentially with the DC bias voltage across the defective capacitor. The I-V characteristics are symmetric with voltage and independent of the polarity of the ESD discharges. A simplified model consisting of two diodes in parallel in opposite directions is proposed to represent the DC behavior of the defective capacitors.

1. Introduction

Multi-layer ceramic (MLC) capacitors are widely used in modern electronic devices, especially in automotive electronics due to their high reliability, small size and low cost compared to other types of capacitors. With the increasing demands for a high-level of product integration and component miniaturization, MLC capacitor design is evolving and newer capacitors are made with ceramics that have a higher dielectric constant, they have an increasing number of stack layers, increasing overlap area between internal electrodes and thinner dielectric layers [1]. The new materials and closer electrode spacing is resulting on an increased focus on the effects of electric overstress (EOS) such as electrostatic discharge (ESD). Also, the use of these capacitors in safety-critical systems has generated interest in modeling their electrical behavior after a failure has occurred.

In earlier work examining the failure of MLC capacitors, efforts have been mainly focused on the mechanical overstress (MOS) [2] and highly accelerated life tests (HALT) [3], [4], [5]. During HALT testing, ceramic capacitors experience degradation not only in their capacitance, but also in their insulation resistance due to Schottky barriers formed between the dielectric material and electrodes [6] and oxygen vacancies [7].

ESD is always an important consideration when designing any electronic component or device that will perform a safety-critical role. However, the failure of the capacitors under ESD stress has not been widely documented. Only a few published studies have investigated failures or degradation of MLC capacitors under ESD stress. One of these studies, [11], stated that the rate of failure (defined as not meeting the initial resistance requirements) increases with an increase in the cumulative voltage on the capacitor. In this study, 1000 X7R capacitors (0805 1-nF and 1206 10-nF) were tested with 5 8-kV ESD strikes in each polarity. No charges were accumulated before the next strike. The authors found no significant difference when testing with a human body model (150-pF/1500-ohm) network or a machine model with a 200-pF capacitor. The study described in [8] was a further investigation of [11], indicating that a higher breakdown voltage improved immunity to ESD in the capacitors they tested. In [12], a continuous ESD test of 10 strikes followed by another 10 strikes with reverse polarity at a frequency of 10 Hz was used to characterize NP0/X7R MLC capacitors with 50-V or 100-V ratings and packages sizes from 0402 to 0805. Failures were determined by a test sample's inability to meet capacitance, dissipation factor or IR requirements. It was found that higher voltage rated parts outperformed the lower rated ones and larger case size parts outperformed smaller ones. In [9], a degradation in capacitance was identified by gradually increasing the ESD level from +/- 0.5 kV to +/- 5.0 kV in intervals of +/- 0.5 kV. In [10], resistive shorts occurred in 0603 MLC capacitors with nominal

values of 680 pF and 10 nF subjected to a 15-kV ESD test. That paper proposed a model employing a shunt resistor together with a capacitor to represent the defective capacitor. The assumption for the "resistor model", however, could only be applied to situations where the DC bias voltage was constant; and it fails to account for other possible DC bias voltages which may be applied on the capacitor. Also, the paper did not explore the ESD levels at which these capacitors were degraded.

This paper further investigates the degradation characteristics of MLC capacitors caused by ESD stress over a variable DC bias voltage range. The paper starts with descriptions of the test and measurement procedures; then presents failure ESD levels for MLC capacitors from different manufactures and with different voltage ratings. In the following sections, I-V characteristics of defective capacitors are presented and equivalent circuits for a simulation model are proposed.

2. Experiment

2.1 ESD setup and test samples

A human body model (HBM) ESD stress is applied across a MLC capacitor using a 150 pF/330 Ω network configured as indicated in Fig. 1. A contact ESD is used to minimize the variation of energy passing through the capacitor. The capacitor is covered with silicone gel to avoid an air discharge across terminals of the capacitor or surface discharge along the capacitor body.

In this test, MLC capacitors with rated values of 1 nF, 10 nF and 100 nF were obtained from three manufacturers. All capacitors in this study were type II X7R capacitors with 0603 packages and 50-V ratings. Tests were conducted on 8 samples of 1-nF and 10-nF capacitors and 3 samples of 100-nF capacitors.

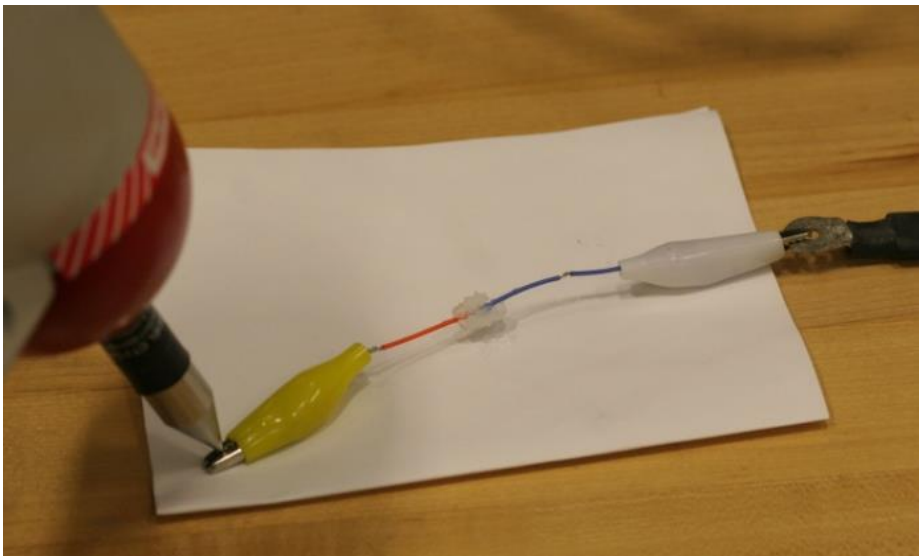

Fig. 1. ESD setup with a capacitor under test covered with silicone gel.

2.2 ESD sequence and measuring procedure

A single contact ESD was applied to the capacitor under test (CUT) starting with a voltage level that was not likely to destroy the test sample. These starting voltage levels were determined by trial tests, in which, no samples were damaged by a single strike at a given ESD level, for example, +2 kV for 1-nF capacitors. The voltage level was increased in steps of either +1 kV or +2 kV (Table 1) to determine the failure voltage level for each capacitor.

Table 1: Test sequence for capacitors with different voltage ratings

Step	1 nF	10 nF	100 nF
1	+2 kV	+8 kV	+18 kV
2	+3 kV	+ 9 kV	+20 kV
3	+4 kV	+ 10 kV	+22 kV
4	+5 kV	+ 11 kV	+24 kV
5	+6 kV	+ 12 kV	+26 kV
6	+7 kV	+ 13 kV	+28 kV
7	+8 kV	+14 kV	+30 kV
8	+9 kV	+15 kV	-
9	+10 kV	+16 kV	-
10	+11 kV	+17 kV	-

After each test, the DC resistance of the capacitor is measured using an LCR meter. The capacitor was considered to be damaged if the measured resistance was less than 10 MΩ. If it was not damaged, the test was continued at the next voltage level, and this was repeated until the capacitor was damaged. For example, on a 1-nF capacitor, the test was started at 2 kV and incremented in steps of 1 kV until reaching the observed failure voltage level between 4 kV and 7 kV. The defective capacitor was connected to a voltage divider circuit, as shown in Fig.2. The DC voltage was varied from 0 to +60 V to obtain the I-V curve. The capacitor was tested in both polarities, with the applied voltage represented by the waveform in Fig. 3. The current flow through the sample was calculated using R_2 and the voltage was calculated from V_1 and V_2.

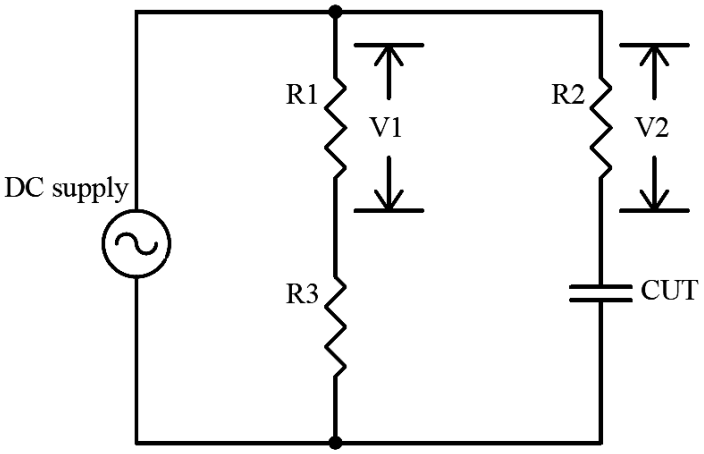

Fig. 2. Test circuit for evaluating degraded capacitors.

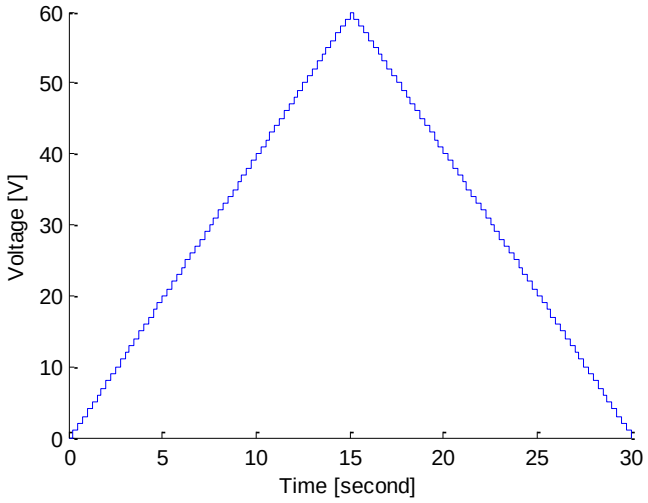

Fig. 3. Applied test waveform from the DC supply.

3. Results and Discussion

3.1 ESD test levels to degrade the capacitors

The failure voltage levels from the ESD tests on capacitors with 1-nF and 10-nF rated values, from different manufacturers are as shown in Fig. 4 and Fig. 5 respectively. The results indicate consistent failure levels of 4 kV and 15 kV for 1 nF and 10 nF capacitors, respectively, from manufacturer B. For manufacturers A and C, there was some variation in the failure levels.

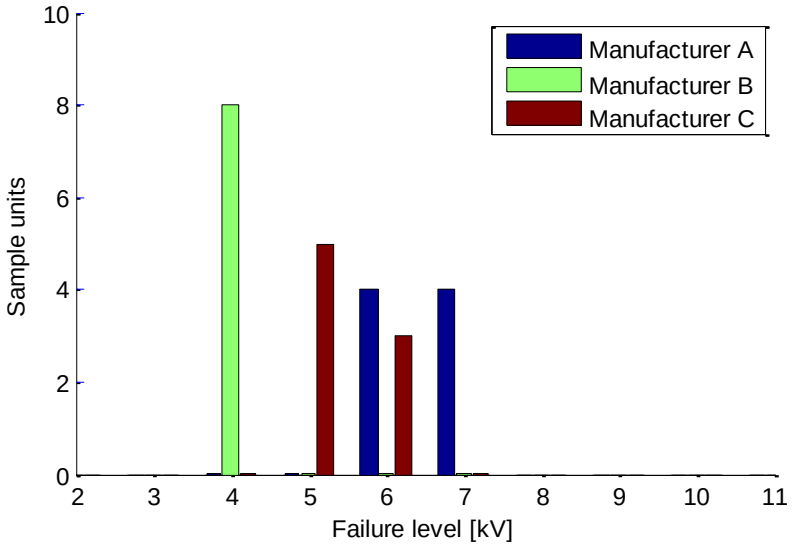

Fig. 4. Histogram of contact ESD failure voltage levels on 1-nF capacitors.

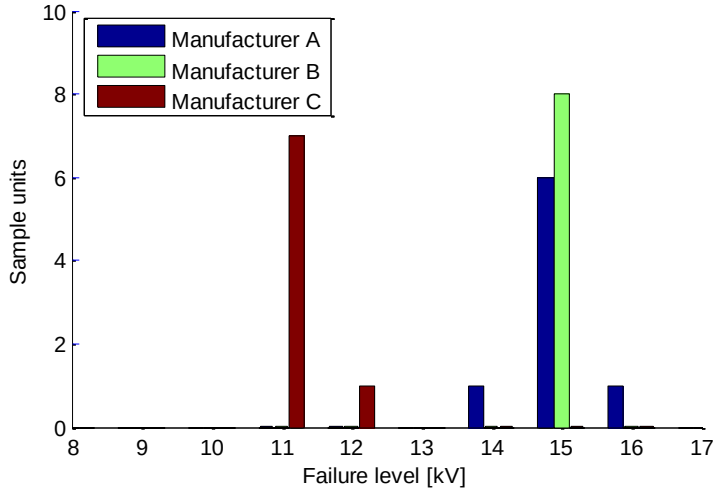

Fig. 5. Histogram of contact ESD failure voltage levels on 10-nF capacitors.

None of the 100-nF capacitors tested were damaged at any level. All of them withstood the maximum 30-kV discharge.

3.2 Non-linear resistive characteristics

The I-V characteristics of damaged 1-nF and 10-nF capacitors are shown in Fig. 6 and Fig. 7, respectively. A non-linear resistance between the capacitor terminals is observed. The symmetry of the plots in Fig. 10 suggests that the failure characteristics of the degraded capacitors are independent of the polarization of the ESD strikes. Comparing Fig. 6 and Fig. 7, it is also worth noting that the 10-nF capacitors from manufacturer C exhibit a much larger leakage current than the other failed capacitors.

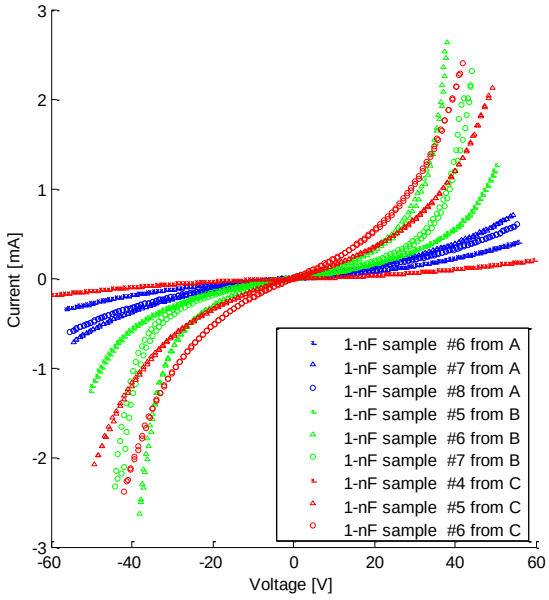

Fig. 6. I-V characteristics of 1-nF defective capacitors.

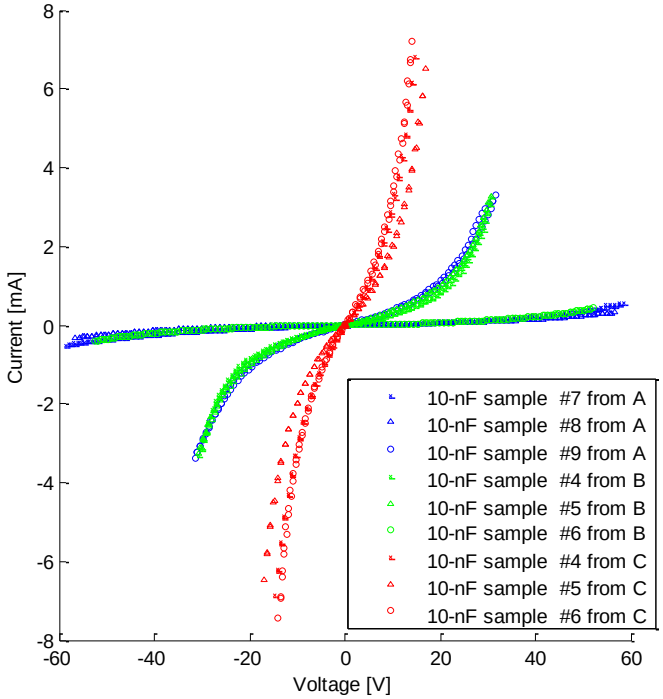

Fig. 7. I-V characteristics of 10-nF defective capacitors.

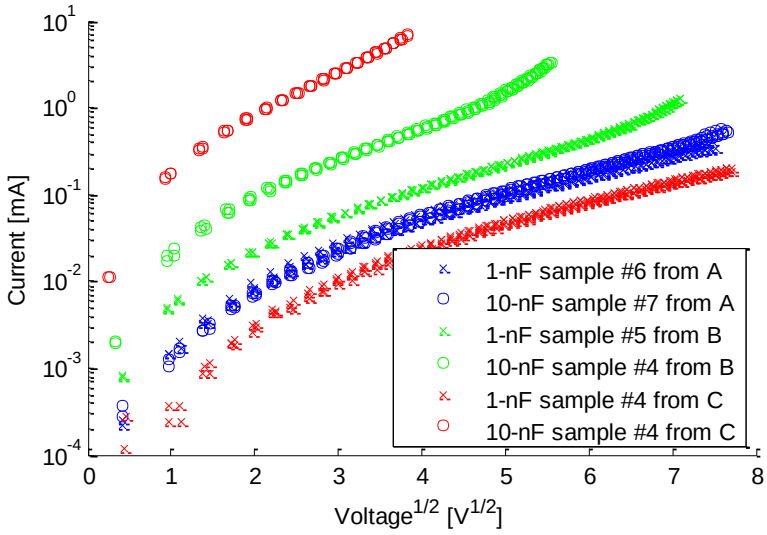

Fig. 8. I-V characteristics of defective capacitors in Schottky coordinates.

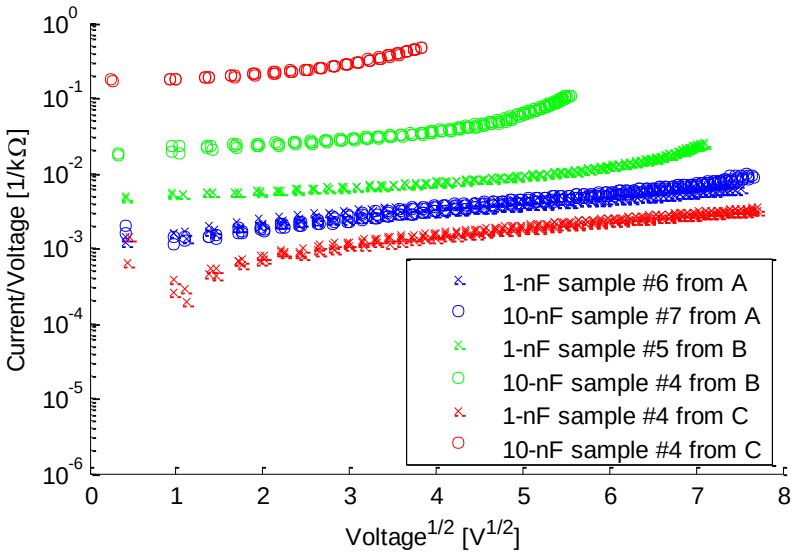

Fig. 9. I-V characteristics of defective capacitors in Poole-Frenkel coordinates.

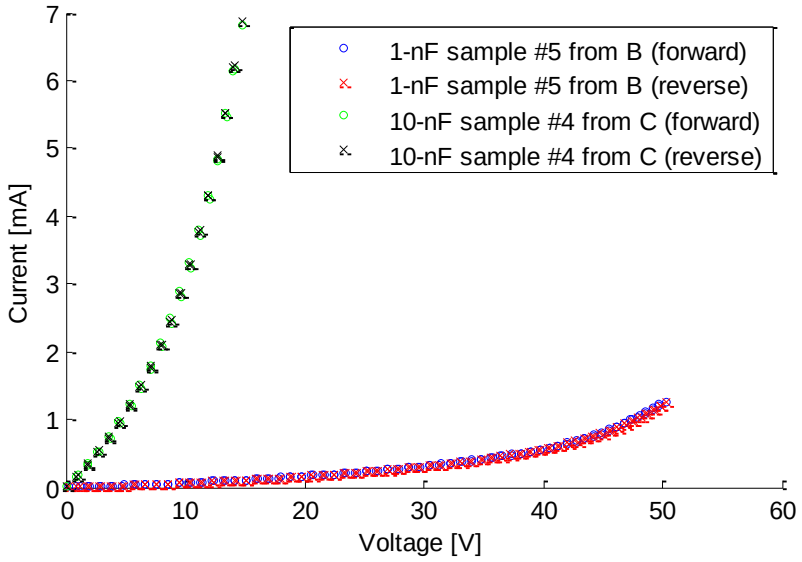

Fig. 10. Symmetric characteristics of the I-V curves.

The conduction mechanism of the defective capacitors can be demonstrated more explicitly by plotting the I-V curve in Schottky coordinates or Poole-Frenkel coordinates, as shown in Fig. 8 and Fig. 9, respectively. The I-V characteristics of these capacitors show decent linearity in both coordinates. Investigation of the conduction mechanism of these degraded capacitors caused by ESD stress is beyond the scope of this paper. However, the results in Fig. 6 and Fig. 7 are consistent with Schottky effects.

3.3 Equivalent circuit of defective capacitors

Observing the physical behavior of defective capacitors as in Fig. 7 and Fig. 8, these capacitors can be modeled as face-to-face Schottky diodes with thermal emission features being applied with reverse voltages. These diodes are modeled in parallel with the defective capacitor. However, a thermionic emission model is not widely used for the Schottky diode model in

SPICE-based software. Considering the exponential increase in current with the increase in applied DC voltage, the behavior of the degraded capacitor, caused by ESD strikes, can be simulated in SPICE with a stack of diodes as shown in Fig. 11.

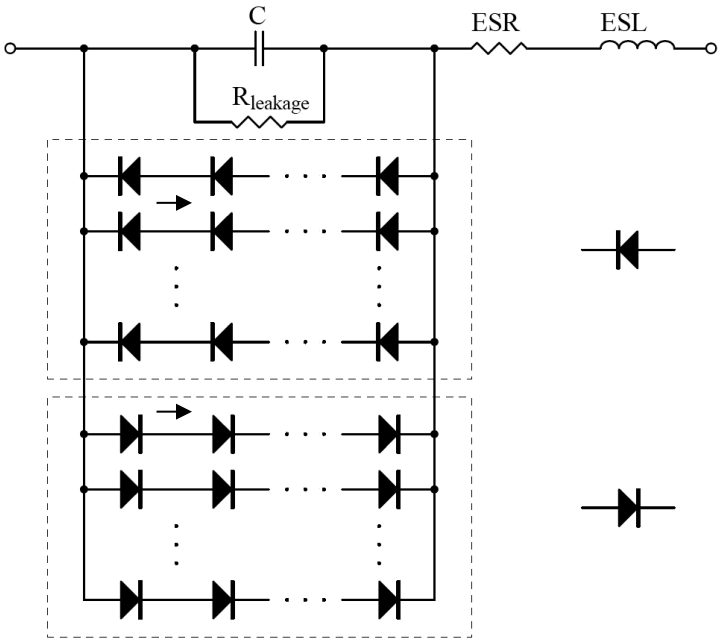

Fig. 11. Equivalent circuit of a degraded capacitor.

At a very low frequencies, the equivalent series inductance (ESL) and equivalent series resistance (ESR) are neglected. For the DC model, the capacitance and $R_{leakage}$ accompanying the capacitor can be ignored. The circuit is then treated as only two diodes. The relationship between the current and the voltage with two ideal p-n junctions can be written as,

$$I = I_S\left(e^{\frac{V}{nV_T}} - e^{-\frac{V}{nV_T}}\right) \tag{1}$$

where I_S is the saturation current of one diode, and V_T represents the thermal voltage, with an approximate value of 25.26 mV at a temperature of 20° C, and n is the emission coefficient. The unknown parameters can be readily modified in a SPICE diode model. As a result of series expansion, Equation (1) can be approximated by eliminating the 2nd-order and higher order components to yield,

$$I \approx \frac{2I_S}{nV_T}V. \tag{2}$$

Thus, the DC resistance R_S with a small DC bias voltage applied is,

$$R_S = \frac{nV_T}{2I_S}. \tag{3}$$

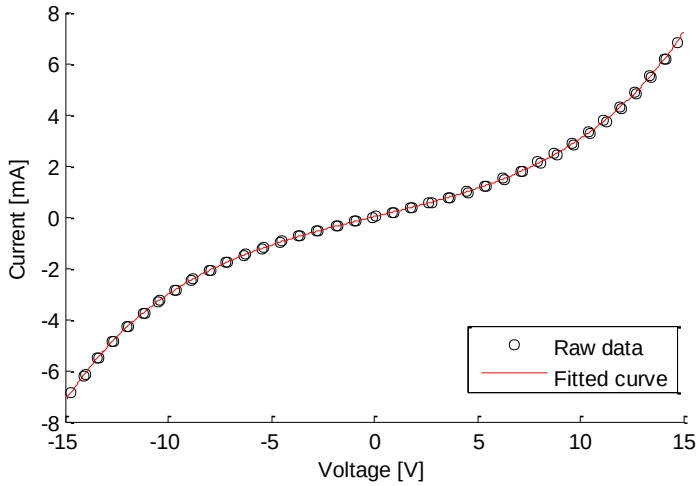

Fig. 12. Curve fit of I-V characteristics for the 10-nF sample capacitor #4 from manufacturer C.

The coefficients, *Is* and *Rs*, for the defective capacitors are derived from the proposed model. Assuming room temperature, the emission coefficient can be obtained using Equation (3). These values for 1-nF and 10-nF capacitors for different samples from each manufacturer are provided in Table 2 and Table 3, respectively. In Fig. 12, which shows the I-V characteristics of the 10-nF sample #4 from manufacturer C, it can be observed that the proposed model is consistent with the measured data.

From the data in Table 2 and Table 3, the graph in Fig. 13 comparing R_S and emission coefficient was plotted to investigate the relationship between them. It can be observed that, 10-nF capacitors have relatively low fault resistances at a small bias DC voltage compared to 1-nF capacitors. There is no obvious correlation between R_S and emission coefficient for the capacitors with the same nominal value.

Table 2: Model parameters (I_S and R_S), model effectiveness (RMSE) and emission coefficient (n) for 1-nF capacitors

CUT	A #6	A #7	A #8	B #5	B #6	B #7	C #4	C #5	C #6
I_S (mA)	0.0477	0.0705	0.0742	0.0394	0.0177	0.0086	0.0244	0.1144	0.1466
R_S (kΩ)	280.0	166.0	176.6	187.1	218.4	463.7	572.2	73.98	51.24
RMSE (mA)	0.0197	0.0074	0.0044	0.0212	0.0757	0.0943	0.0062	0.0139	0.0127
n	1057	927	1038	584	306	316	1105	670	595

Table 3: Model parameters (I_S and R_S), model effectiveness (RMSE) and emission coefficient (n) for 10-nF capacitors

CUT	A #7	A #8	A #9	B #4	B #5	B #6	C #4	C #5	C #6
I_S (mA)	0.0381	0.0200	0.1574	0.0737	0.1197	0.0230	0.5942	0.3906	0.5354
R_S (kΩ)	290.6	503.0	32.60	55.45	39.13	392.2	5.043	7.726	5.044
RMSE (mA)	0.0122	0.0047	0.0639	0.0621	0.0502	0.0061	0.0458	0.0527	0.1424
n	877	797	406	324	371	714	237	239	214

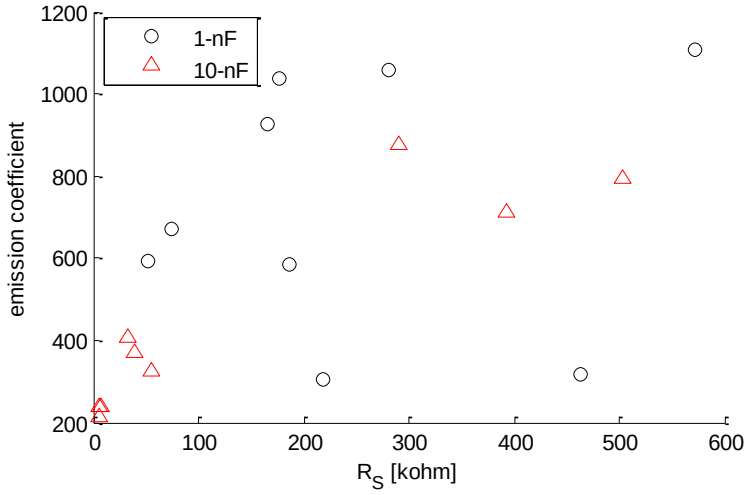

Fig. 13. Emission coefficient vs. R_S.

4. Conclusion

This paper describes and models the degradation of certain MLC capacitors under ESD stress. Two conclusions can be drawn based on these results:

1. For the X7R capacitors evaluated with an 0603 package and 50-V rating, the damaging ESD voltage level for a 10-nF capacitor was higher than that of the 1-nF capacitors tested. ESD strikes up to +30 kV did not cause a failure in the 100-nF capacitors tested.
2. Damaged capacitors exhibited degradation in the insulation resistance. The leakage current flowing through the capacitor increased exponentially with an increase in the applied DC voltage. The I-V curves for the degraded capacitors were symmetric with applied voltage and independent of the applied ESD polarity.

The proposed DC model for the damaged capacitor can be readily implemented in circuit simulation software with only two extracted parameters.

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